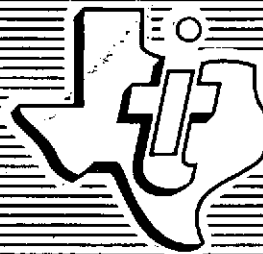(NASA-CR-136936) CHARGE-COUPLED DEVICE IMAGE SENSOR STUDY Final Technical Report (Texas Instruments, Inc.) ~~100~~ p 96

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FINAL TECHNICAL REPORT
CHARGE-COUPLED DEVICE
IMAGE SENSOR STUDY
CONTRACT NO. 953673
3 DECEMBER 1973

Prepared for

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PRICES SUBJECT TO CHANGE

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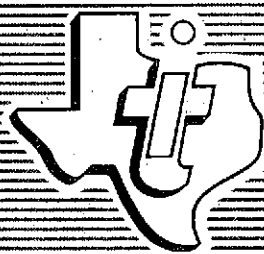
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FOREWORD

In late June of 1973 Texas Instruments began a study of CCD image sensors for the Jet Propulsion Laboratory under contract No. 953673. The study was to investigate the feasibility of using charge-coupled devices for the optical sensors in spaceborne imaging systems and also to formulate recommendations for a CCD design to be developed in a suggested eighteen-month program. This document is the final technical report prepared by Texas Instruments at the end (in late November 1973) of the study program.

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ABSTRACT

This document gives the design specifications and predicted performance characteristics of a Charge-Coupled Device Area Imager and a Charge-Coupled Device Linear Imager that are recommended for development during a proposed 18-month R&D program. The Imagers recommended are intended for use in space-borne imaging systems and therefore would meet the requirements for the intended application. A unique overlapping metal electrode structure and a buried channel structure are described. Reasons for the particular imager designs are discussed.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

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LIST OF ILLUSTRATIONS (Continued)

FINAL TECHNICAL REPORT
CHARGE-COUPLED DEVICE IMAGE SENSOR STUDY
CONTRACT NO. 953673

SECTION I

INTRODUCTION

This final report is one of three documents resulting from a Charge-Coupled Device Image Sensor Study. The other two documents are: "Plan for a Program to Develop CCD Image Sensors" (TI-08-73-61) and "Cost Estimate for Conducting the Program for Developing CCD Image Sensors" (TI-08-73-62). Hence, two programs are discussed and should be differentiated herein: (1) a "Study Program" that is completed with the preparation of these three documents, and (2) a proposed 18-month "Development Program" that is to be completed near the end of the calendar year 1975 with the delivery of CCD Sensors and the demonstration of compliance with specified performance characteristics.

A Charge-Coupled Device Area Image Sensor consisting of a two-dimensional array of charge-transfer, MOS capacitors, and ancillary circuits will be referred to in this report as the Area Imager; and a Charge-Coupled Device Linear Image Sensor consisting of a one-dimensional array of MOS capacitors and ancillary circuits will be referred to as the Linear Imager. A particular Area Imager and a particular Linear Imager, both of which will be described in detail in Section II of this report, are recommended for development during the Development Program. Both Imagers are intended for use with space-borne instruments.

The specifications for both Imagers have resulted from the Study Program and represent a considered judgement of devices that can both be manufactured during the alloted time period and meet the application requirements. We believe that the development of a 500 by 500 element, or larger, Area Imager should be conducted in two successive programs. The first program should develop an Area Imager that is as large (approximately 400 by 400 elements) as can be fabricated while using photomasks produced from a single reticle. The development of larger Imagers requiring photomasks produced by reticle composition should be done in a subsequent program. (Development of the larger imagers is not discussed in this report.) Although our judgement was weighted heavily by considerations of photomask production and reticle composition factors it was not based entirely on these factors as our discussion of the various problems of Area Imager fabrication in this report shows.

The following objectives of the Study Program apply to the Area Imager and to the Linear Imager:

(1) To examine the performance goals given in the Study Guidelines (Attachment 1 to Contract No. 953679, March 2, 1973), and by studying the various kinds of CCD's, making theoretical analyses, and conducting experiments to describe a hypothetical CCD that would most nearly meet all performance characteristics required for the intended application.

(2) To examine the requirements for developing the CCD described in (1) and to determine the changes that would have to be made to ensure success during the Development Program.

(3) To effect the most reasonable compromise between the "goals" and "success."

(4) To specify the design of the resulting proposed CCD image sensors.

The final objective was to prepare the three documents described above.

The specified Imagers are described in detail in Section II of this report. The expected performance characteristics of the Imagers are discussed in Section III. In Section IV, reasons are given for choosing the particular electrode and channel structures, configuration, scanning mode, and other design and operational features.

SECTION II

RECOMMENDED DEVELOPMENT MODELS SPECIFICATION

In the following paragraphs the recommended Area Imager and Linear Imager are described. Reasons for the design choices are given in a separate section.

The Area Imager will be a cooled, full frame, three-phase, buried channel device; it will be mechanically shuttered; and it will have an $A\ell$-$A\ell_2O_3$-$A\ell$, overlapping electrode structure. The Linear Imager will be cooled and electronically shuttered; it will be a three-phase, buried channel device; and it will have an $A\ell$-$A\ell_2O_3$-$A\ell$, overlapping electrode structure. The Linear Imager chip will also contain a storage buffer providing rapid readout of data from the sensor into storage and slow readout of data from storage for transmission.

A. Area Imager Geometry

The recommended Area Imager will have 400 x 400 elements, or pixels, each of which will be 22.9 μm by 22.9 μm (0.9 mil by 0.9 mil) in size. The size of the sensor matrix alone would then be 9.1 mm by 9.1 mm (0.36 inch by 0.36 inch); this would also be the size of the backside thinned area. On the frontside, space must also be provided for clock drive lines and interconnections to electrodes, the horizontal serial register, and its clock lines for readout, and the bonding pads. See Figure 2-1. To facilitate thinning and mounting, the bonding pads will need to be set further away from the active chip area than is usual for MOS devices. Consequently, the overall chip area will approach a 12.5 mm (0.5 inch) square. The Area Imager will be a three-phase device such that three parallel metal electrodes per pixel height will run "horizontally" across the "vertical" buried channels of the array.

B. Linear Array Geometry

The recommended CCD Linear Array will have 150 x 1 elements, each of which will be 22.9 μm x 22.9 μm (0.9 mil x 0.9 mil). The Linear Imager will actually be a 100 x 150-element area imager with all but one row of horizontal pixels masked by an opaque overcoating such as aluminum. The 100 x 150-element area imager will meet all specifications (except the number of elements) for the 400 x 400-element Area Imager. The exposed row of pixels constitutes the 150-element Linear Imager. The masked part of the array constitutes the storage buffer. Hence, data can be read out of the linear imager into the storage buffer at a rapid rate and later read out of the buffer for processing or transmission at a slower rate.

C. Electrode Structure

The aluminum-aluminum oxide-aluminum, overlapping gate structure will be used; a cross-section of such a structure is illustrated in Figure 2-2. Each electrode length is 7.4 μm (0.29 mil). The electrode separation is the thickness of the anodized layer, which is approximately 0.3 μm (0.01 mil).

CHANNEL STOP DIFFUSION

ONE PIXEL ELEMENT

FAT ZERO
REFERENCE DIODE

FAT ZERO
LOAD
GATE

ϕ_1

ϕ_2

ϕ_3

PARALLEL-
SERIAL
TRANSFER GATE

VIDEO
OUT

ϕ'_1

ϕ'_2

ϕ'_3

SERIAL REGISTER

OUTPUT
GATE
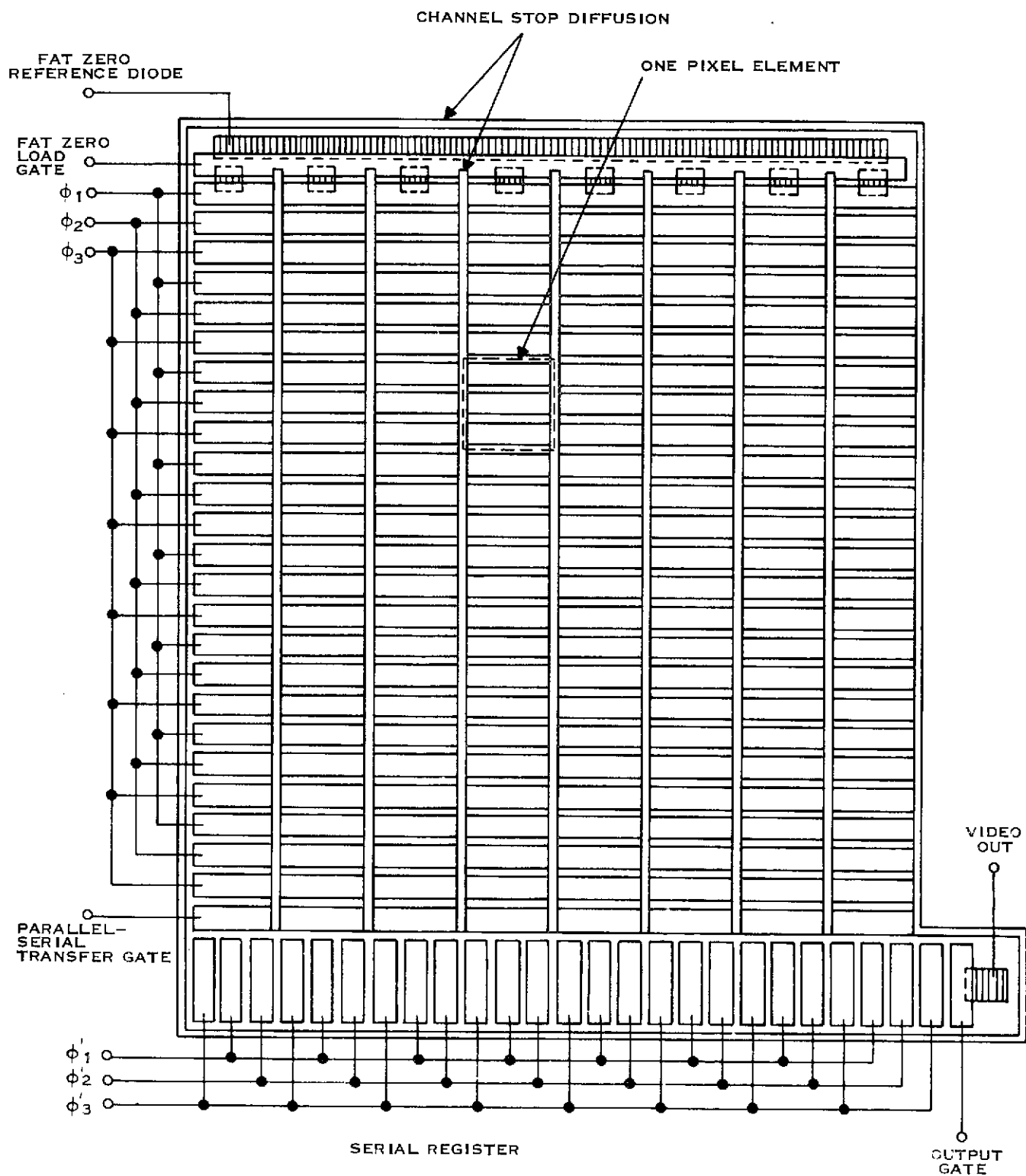
Figure 2-1. Schematic for a Three-Phase, Full Frame, Serial Readout CCI
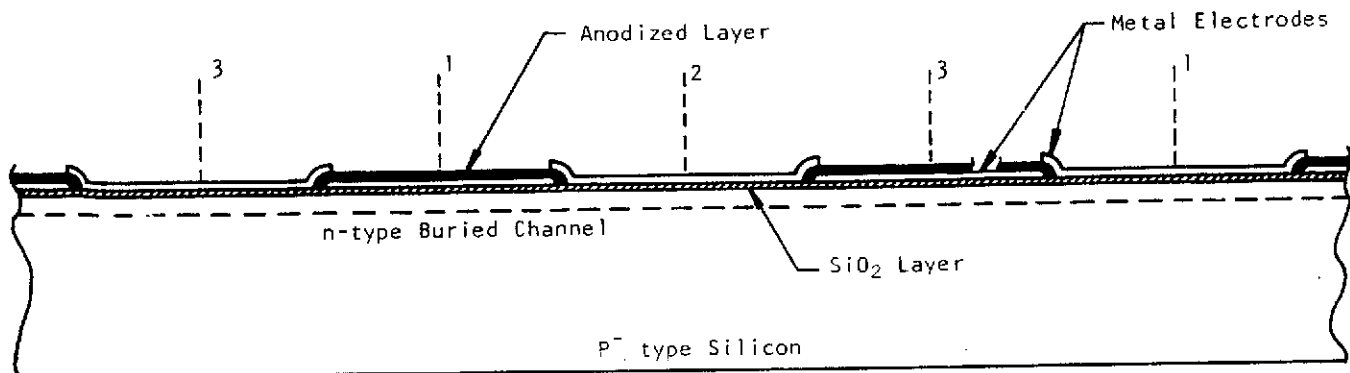
Figure 2-2. Section Illustrating Overlapping Electrode Structure

D. Channel Structure

The vertical channels will be n-type buried channels provided by an ion implantation (phosphorus, $10^{12}/cm^2$), and each would be 17.8 μm (0.7 mil) wide. Channel stops 5.1 μm (0.2 mil) wide produced by a p-diffusion will separate the channels.

E. Thinning — Backside Illumination

To provide for backside illumination, the Imagers will be thinned to a 10 to 12 μm thickness over the area opposite the matrix area. The backside surface will be flat to 0.02 mm over the thinned area.

F. Antireflection Coating

The thinned area on the backside will be treated for minimum reflection at 0.8 μm by coating with a single layer 0.105 μm of SiO.

G. Scanning Mode

The full frame Area Imager will be read out by clocking the 400 vertical channels downward in parallel a pixel at a time to load the horizontal serial register. Between each step of vertical pixel transfer, the serial register will be clocked out through a precharge amplifier. See Figure 2-1. There are, therefore, 4.8 x 10^4 clock pulses required to readout the complete array. At 3 x 10^4 sec^{-4} clocking rate, the readout time would be 1.6 sec.

H. Mounting

Backside illumination, thinning to approximately 11 μm, and the flatness (0.02 mm) required of the thinned surface will bring into being special problems. Consequently, experiments on thinning are proposed during the first six months of the Development Program. An optimum means of bonding the chip to a rigid disk, perhaps a ceramic, before thinning, in order to control the surface flatness better, will be developed during these experiments.

I. Raw Silicon Specification

The Imagers will be fabricated on p-type, <100> boron-doped, 40 ohm-cm, silicon slices that have passed standard acceptance tests.

J. Extra-Array On-Chip Circuits

As Figure 2-1 illustrates, the extra-array circuits are: 1) bonding pads with connecting leads to clock lines, 2) clock lines for both the sensor array and the serial read-out register, 3) interconnections between clock lines and electrodes including vias and tunnels as required, 4) fat zero input diodes and gate, 5) and output gate and precharge amplifier including output gate and drain voltage leads and signal output lead to bonding pads.

The only part of these extra-array circuits that needs to be specified here is the output gate and precharge amplifier, which is also referred to as the floating diffusion amplifier and as the source follower amplifier. This amplifier is currently in use on several Texas Instruments CCD Imagers and has already been described in several documents. The amplifier is shown schematically in Figure 2-3, the semiconductor structure at a, and an equivalent circuit at b.

The precharge amplifier was specifically developed to take advantage of the low output capacitance of the CCD Imager, which with the precharge amplifier can be as low as 0.07 pf. Thus, the amplifier performs the function of removing the charge packets from the array while contributing an extremely low noise level to the signal. Responsivities on the order of 2 μv per electron are routinely achieved. The preamplifier noise (see Appendix C) with the precharge amplifier is equal to

$$n_{out} = \sqrt{2kTC/3q^2}$$

where k is the Boltzmann constant, T is temperature in K, and f is the charge per electron.

K. Power Requirements

Recent experimental work at TI with buried channel CCD's indicates that these devices will operate with quite low clock voltages. It is specified that the Imagers shall operate with clock pulse amplitudes less than 10 volts. The optimum operating voltage will depend on the precise details of device manufacture, and a better estimate of this value must await the fabrication of prototype devices during the first six months of the Development Program.

(A) SEMICONDUCTOR STRUCTURE

(B) AN EQUIVALENT CIRCUIT
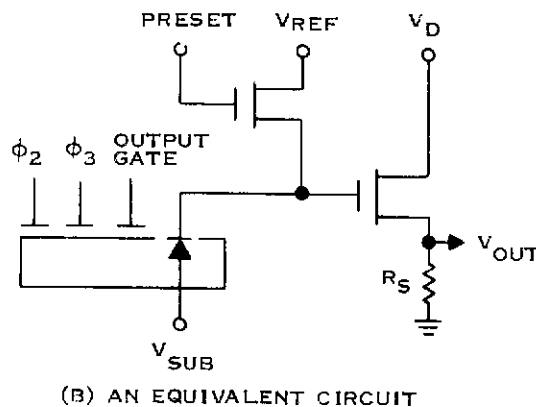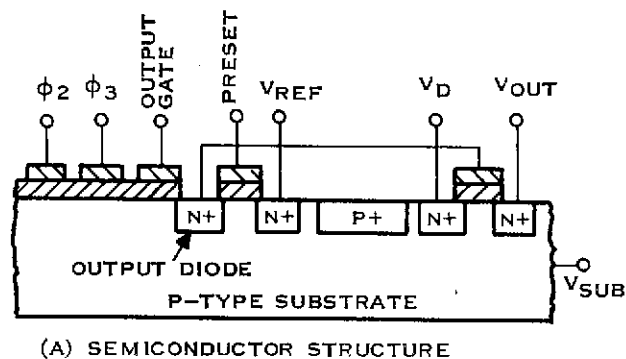
Figure 2-3. Schematic of a Precharge Amplifier

The waveforms applied to the sets of electrodes will be the common 3-phase clocking sequence described in Appendix A. The logic required for precise synchronization of parallel register clocking with that of the output serial register will depend on the details of the array design, and will be finalized during the Development Program.

The Imagers will be capable of operating (when cooled to -40°C) at output pixel rates ranging from 10^4 to 10^6 sec^{-1}. These low data rates will allow the use of complementary MOS (CMOS) logic circuits for reduced power consumption. It may also be possible to drive the sensor directly from the CMOS gates, resulting in further reduction of power requirements. The precise determination of power consumption must await the testing of prototype imagers during the Development Program.

SECTION III
PREDICTED PERFORMANCE CHARACTERISTICS

A. Spatial Resolution – MTF

The discussion of modulation transfer functions which follows for a CCD image sensor will show that the aperture MTF is the most significant source of MTF rolloff in a properly-designed CCD imager. It will also be shown that the transfer efficiency must be at least as high as 0.9998 or the transfer MTF alone will degrade the device MTF to less than 60 percent relative frequency response at 20 line pairs per mm. The value of 0.60 for MTF is of particular interest because this is approximately the maximum MTF that could be achieved at 20 lp/mm with the proposed sensor, if the aperture MTF contained no diffusion factor. Because of diffusion effects, this value is not practically realizable, and a goal of 0.50 for sensor MTF at 20 lp/mm is adopted.

1. Definitions

Spatial Frequency Response in optical and image reconstructing devices is generally expressed as a modulation transfer function (MTF), which relates contrast in the image to contrast in the object at each spatial frequency. "Contrast" used in this context is modulation contrast defined by the equation:

$$C_M = (E_{max} - E_{min}) / (E_{max} + E_{min}), \tag{1}$$

where E is illuminance (lumens/cm^2). When illuminance is expressed as a cosine function of spatial frequency, that is,

$$E = a + b \cos 2\pi \nu x, \tag{2}$$

with $a \geqslant a \geqslant 0$, the modulation contrast is (b/a). The spatial frequency response at the frequency ν is

$$R_\nu = (b'/a') / (b/a), \tag{3}$$

where the primed and unprimed symbols represent image quantities and object quantities respectively. A plot of R_ν versus spatial frequency is the MTF.

With respect to a CCD image sensor, it is assumed that the sensor is used to extract information from a primary image and that the data obtained is subsequently used to reconstruct a secondary image. Within the system that processes the extracted information and displays the reconstructed image, a contrast can generally be recovered from the data being processed at several stages in the system including the ultimate stage, the display. An MTF for that part of the system between the primary image and a particular stage is the contrast at that stage compared with the contrast in the primary image.

The sensing of an optical image by a Charge Coupled Imager is a two-dimensional sampling process. From the theory of sampling, we know that aliasing will occur if the image (the function being sampled) contains spatial frequencies higher than a certain frequency, called the Nyquist frequency v_N, that is related to the spacing ℓ between sampling points. That is,

$$v_N = 1/2\ell .\tag{4}$$

Frequencies higher than v_N do not appear in the image ideally reconstructed from the sampled data. However, aliasing causes a portion of the radiant power that belongs to frequencies in the primary image higher than v_N to be added, in the reconstructed image, to frequencies that are lower.

In an Area Imager, two directions for spatial frequencies need to be distinguished. The Nyquist frequencies will differ if the pixel spacing is different since a pixel spacing is the same as sample point spacing. Also, because of the way the data is read out and processed, the MTF may differ with direction. Hence, we specify a vertical direction and a horizontal direction. To agree with conventional usage in the language of TV engineering and the TV mode of scanning an image, the vertical direction (with a corresponding vertical MTF) is the direction of a channel in the active sensor region or the direction perpendicular to the metal electrode stripes. The horizontal direction is parallel to the electrode stripes and also the direction of the serial readout register channel. Hence, one "horizontal" row of pixels corresponds to one scan line of a conventional TV raster.

2. Aperture MTF

A region on the surface of the CCD defines an aperture for each pixel. The aperture includes all of the surface area such that for each photon incident on the area there is a finite probability P that an electron will appear in the potential well of that pixel. Let us study a simple case first, one that would apply for backside illumination.

If the aperture is a rectangle with sides x_1 and y_1, with x_1 being the horizontal side, the aperture function is defined by the rectangular function

$$P_r = C, \text{ when } - (x_1/2) \leqslant X \leqslant (x_1/2)$$

$$\text{and } - (y_1/2) \leqslant y \leqslant (y_1/2),\tag{5}$$

$$P_r = 0, \text{ when } |x| > (x_1/2) \text{ or } |y| > (y_1/2) .$$

where C is a constant. The aperture MTF would then be

$$(MTF)_r = Cx_1 y_1 \text{ sinc } \pi v x_1 \text{ sinc } \pi v y_1 ,\tag{6}$$

$$\text{where sinc } \pi v \ x_1 \equiv (\sin \pi v \ x_1) / (\pi v \ x_1) .$$

The aperture MTF is usually taken to be that for the rectangular aperture with x_1 and y_1 being the horizontal and vertical dimensions respectively of a pixel. However, this could involve a significant error with frontside illumination, particularly if the electrode and channel structures are such that light must find its way through an opening that is smaller than the pixel size. The sinc function goes to zero when its argument is equal to π, that is when

$$\nu_{xc} = 1/x_1 . \tag{7}$$

Let us set x_1 equal to some fraction m of ℓ. Then, we have:

$$\nu_{xc} = 1/m\ell = 2\nu_{Nx}/m . \tag{8}$$

Therefore, when m is less than unity, a significant portion of the aperture spatial frequency bandpass extends beyond the Nyquist limit and aliasing will occur.

The proposed area Imager with its pixel spacing $[x_1 = \ell = (1/22_\eta)]$ of 22.9 μm has a Nyquist limit ν_N of approximately 22 line pairs per mm which is indeed greater than the cutoff frequency (20 mm/^{1}) implied by the guidelines. The argument of the sinc function at 20 mm^{-1} has the value $\pi 20\ell = [\pi(10/22] \approx 1.428$ radian. The sinc function for this argument has a value approximately equal to 0.69, that is, this is the aperture MTF at 20 line pairs per mm, assuming that lateral diffusion of carriers in the silicon substrate has no effect on the MTF.

3. Transfer Inefficiency MTF

The small portion of charge that is left behind at each transfer causes a degradation of the MTF for the CCD sensor. The frequency response as a function of spatial frequency (the MTF) has been shown to be (see references 61 and 68)

$$(\text{MTF})_\epsilon = \exp \{ -n_\epsilon [1 - \cos (\pi\nu/\nu_N)] \} , \tag{9}$$

where n is the total number of transfers and ϵ is the transfer inefficiency defined as the fraction of the charge packet left behind at each transfer. A plot of $(\text{MTF})_\epsilon$ is shown in Figure 3-1. In addition, the output signal experiences a frequency-dependent delay resulting in a phase shift of $n\epsilon \sin (\pi\nu/\nu_n)$. Distortion in the image can result from the delay caused by a too-large $n\epsilon$ product.

Let us find what transfer efficiency is needed to achieve an MTF of 0.60. The argument of the cosine of Equation 9, for a spatial frequency equal to 20 mm^{-1}, is $\pi(20/22)$ and the cosine itself is -0.95949 so that

$$(\text{MTF})_{\epsilon 20} = \exp (-1.959 \, n\epsilon) > 0.60 , \tag{10}$$

or

$$1.959 \, n\epsilon < 0.51 , \tag{11}$$

$$n\epsilon < 0.26 .$$

In the recommended 3-phase 400 x 400 Area Imager, a maximum of 1200 transfers are required vertically downward, and a maximum of 1200 to transfer out of the serial register. The computed, required transfer efficiency must be at least 0.99978 in each direction or else the MTF caused by transfer inefficiency alone will be less than 0.60.

Since the ideal aperture MTF is 69 percent, it is of interest to find what efficiency is required for the transfer MTF to be not less than (60/69) or 0.87, which would reduce the combination MTF to 60 percent. It is 0.999941, which is very high, but, according to recent experimental results, still an achievable goal.

B. Gamma

The response of a Texas Instruments CCD area imager (a single-metal-level, 3-phase, 100 x 150 element device) has been measured with a range of illumination levels. A plot of the current response as a function of illumination level, as shown in Figure 3-2, shows the gamme to be unity.

Figure 3-1. Modulation Transfer Function Resulting From a Charge Transfer Inefficiency For a Charge-Coupled Image Sensor (Reference 61)

C. Spectral Response

The spectral response of a Texas Instruments CCD imager has been measured and the relative response is shown in Figure 3-3. The device was illuminated on the frontside. A relative spectral response of a silicon vidicon (TI Tivicon) is also shown for comparison. The structure in the CCD curve near 0.70 and 0.80 μm and the rolloff in the near infrared are caused by dielectric layers of SiO_2 and Si_3N_4 on the frontside. With backside illumination and with the surface properly coated for antireflection, the spectral response of the CCD should more closely resemble that of the silicon vidicon. Even the wavelength at which the response peaks can be adjusted over a narrow range of wavelengths.

D. Dynamic Range

Measurements of noise equivalent power on a 100 x 150 area array at TI have yielded a value as low as 3.45 x 10^{-9} W, for a 2854 K source. The responsivity of the device was 8.7 x 10^{-3} A/W, so the noise equivalent rms number of noise electrons per pixel, using the (essentially continuous) output clock rate of 300 kHz, this quantity is found to be 625 electrons. The capacity of a single electrode in this device was about 5 x 10^6 electrons with the clock voltage used (12 V). Thus, the measured dynamic range was 8000:1.

Figure 3-2. Response of a TI Charge-Coupled Area Imager as
Function of Illumination Level in Watts From a 2854
K Source Incident on a 0.139 cm^2 device

It is likely that the bulk of this noise was caused by trapping in fast interface states, as the device was a surface-channel CCD. A buried-channel imager will not contain this noise source. On the other hand, the charge-carrying capacity of a buried-channel device is somewhat lower than a surface-channel device of the same geometry. If we assume that the buried-channel imager will be limited by output amplifier noise, a value of 100 noise electrons is reasonable. The full-well charge level for a buried-channel imager of the same geometry as the 100 x 150 would be about 3×10^5 electrons with 12 V clocks. Thus, the dynamic range for such a buried-channel imager should also be about 8000:1.
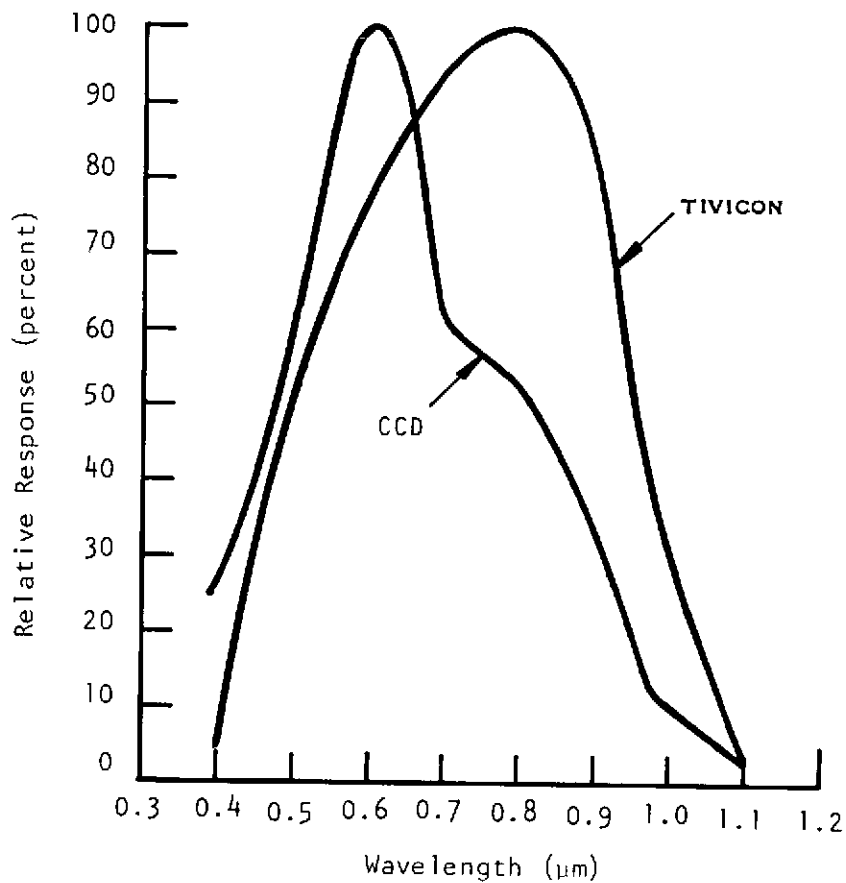
Figure 3-3. Relative Spectral Response of a TI Charge-Coupled Area
Imager and of a TI TIVICON*

E.   Residual Image

Since charge in the depletion regions of a CCD imager is very efficiently transferred from its initial position to the output of the CCD, a residual image could be formed only by charge remaining in the neutral bulk, where it is unaffected by clocking of the electrodes. Thus, the question of whether there will be a residual image hinges on the value of the time constant for charge to remain in the neutral bulk. The minority carrier lifetime in very pure, bulk silicon can be on the order of a millisecond before processing to fabricate a CCD. However, after processing, the lifetime will generally be less than 100 microseconds. Thus, if the frame time of a CCD imager is greater than, say, 300 microseconds, there can be no appreciable residual image from one frame to the next.

*Trademark of Texas Instruments Incorporated.

3-6

Since the CCD sensor will be of a finite thickness, the time constant for removal of minority carriers from the neutral bulk will actually be considerably shorter than 100 microseconds. Since the depletion region at the surface of the CCD keeps the minority carrier density at the depletion region-neutral bulk interface very low, diffusion to the depletion region from the bulk proceeds at a rapid rate. For example, if the thickness of the neutral bulk is 5 mils, the time constant for diffusion of electrons to the depletion region in high-quality silicon will be about 2 μsec. If the substrate of the imager is thinned to 12 μm, the time constant for diffusion from the bulk is only about 10 nsec. For such a thin substrate, therefore, not only will there be no residual image from frame to frame, but there will be no smearing of the image caused by residual image from element to element during shift-out.

Conceivably, in a relatively thick substrate (≈ 10 mils), element-to-element residual image could cause image smearing, or decreased MTF. In the Area Imager operated with mechanical shuttering, this effect could be prevented by delaying shift-out for a few microseconds after closing of the shutter. Even in an Area Imager operated with electronic shuttering, the ratio of integration time to diffusion time constant can be made long enough that residual image will cause no significant degradation in MTF. In a scanned linear array this might not be the case, if the substrate is thick enough and the line integration time short enough. For example, the diffusion time constant for a 10 mil-thick substrate is about 8 μsec. In a linear imager with buffer storage, the integration time per line could be made this short. For a substrate thinned to 12 μm, however, even the linear array should suffer no loss in MTF caused by residual image.

F. Blemish Count

Blemishes will affect yield during device fabrication; and a count of blemishes is one criterion for accepting or rejecting fabricated devices. Blemishes, as defined in the next sentence, on acceptable devices will not exceed two entire lines plus 50 additional pixel elements. A blemish is defined as an output signal variation equal to 20 percent of the output at nominal saturation exposure amplitude when the sensor is unilluminated or when the sensor is exposed to a uniform field that produces nominal saturation amplitude. Nominal saturation exposure is defined as that highlight exposure at which gamma is 0.8.

G. Signal And Dark-Current Uniformity

The signal response at 36 different pixels of a 100 x 150 imager fabricated at TI were measured to obtain an estimate of the nonuniformity of response. The sample standard deviation was 2.8% of the sample mean, at an exposure level of about 50% of saturation. It is anticipated that percentage nonuniformity of response will be relatively independent of exposure level, as it is probably caused by variations in metallization geometry from electrode to electrode, variations in transmission of insulator layers at the surface, and so forth.

Dark current nonuniformity was measured at 41 pixels of the 100 x 150 imager, and found to have a sample standard deviation of 9.6% of the sample mean at a sensor temperature of 300K. Cooling the sensor to 233 K (-40°C) will substantially reduce the magnitude of dark current, though of course the percentage variation in dark current may not be appreciably changed.

The above values for signal and dark current uniformity are probably fairly representative of what may be achieved with other types of CCD imagers, such as thinned, backside illuminated

sensors. The uniformity of response will in fact probably be better in a backside-illuminated imager, because the incident light no longer must pass through gaps between electrodes, or through non-optimum layers of dielectric material at the silicon surface.

H.   Sensitivity: Signal-To-Noise Ratio

The noise levels measured on TI 100 x 150 imagers have already been cited above in the discussion of dynamic range. The responsivity to 2854 K radiation of the device referred to in that discussion was 8.7 x 10^{-3} A/W. Using the area of a single pixel of that device (9.3 x 10^{-10}), one can calculate that an exposure of 100 $\mu j/m^2$ would result in the production of about 5050 electrons per pixel. As the effective rms number of noise electrons was 625, the signal-to-noise ratio for this exposure level would be about 8.1:1.

However, this device was a single-level metal CCD, illuminated from the frontside. Consequently, about 75% of the incident radiation was blocked by the metal electrodes, and additional light was lost through reflection and absorption in the layers of Si_3N_4 and SiO_2 at the sensor surface. Even without special antireflection coatings, a backside-illuminated CCD would be expected to be about four times as sensitive with the same pixel area. The area of a pixel in the proposed sensor is a factor of 0.56 smaller than in the 100 x 150 array. Thus, it is predicted that the recommended sensor will have a signal-to-noise ratio of at least 18:1 at an exposure of 100 $\mu J/m_2$, from a 2854 K source.

I.   Low-Light-Level Performance

The sensitivity of the proposed sensor has been discussed in Section III.H. There it was estimated that the ratio of peak signal to rms noise at an exposure of 100 $\mu J/m^2$ would be greater than 18:1. If we make the assumption that in order to resolve a test pattern consisting of alternating black and white bars, the eye needs a signal-to-noise ratio of about 3, integrated over a bar pair of the test pattern and over about 0.1 second eye integration time, a criterion that has been experimentally verified by Rosell and Willson[*], we find that the proposed sensor should resolve to the Nyquist limit down to a sensor irradiance of about 5 x 10^{-5} W/m² for a noise level of 625 electrons per pixel. This computation is based on a bar length-to-width radio of 10, and on an assumed CCD responsivity of 0.1 A/W, for which the peak signal to rms noise ratio at an exposure of 100 $\mu J/m^2$ is about 50:1. For a lower noise level, the minimum sensor irradiance will be correspondingly lower.

J.   Long and Short Exposure Times

To obtain exposure times of up to 5 seconds, it will be necessary to cool the sensor, if the blemish count goals are to be met. However, cooling to -40°C should allow exposure times of 5 seconds, and possibly longer, to be used with no appreciable degradation in image quality.

Short exposure times, such as 1 millisecond, will require only some provision, either electrical or mechanical, for limiting the duration of the exposure. It is recommended for the present application that mechanical shuttering be used. This not only simplifies the logic circuitry required

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[*]F. A. Rosell and R. H. Willson, "Performance Synthesis (Electro-Optical Sensors)," Technical Report AFAL-TR-2-279.

to operate the imager, but allows a two-fold increase in the number of pixels that may be incorporated in a CCD sensor chip of a given size, compared to an imager designed to be electronically shuttered. The increase in number of pixels results from the fact that electronic shuttering of a CCD imager requires an on-chip storage buffer, capable of holding one entire field, or frame, of the video data. This storage array occupies essentially the same area on the chip as the imager array, and thus limits the number of pixels that may be included in the imager array for a given chip size.

K. Exposure Time and Data Rate

As mentioned above, cooling the sensor is required in order to achieve long exposure times, because of the degrading effects of dark current. The same mechanism also limits the data readout rate of the sensor to values above some minimum rate, which will be a function of the sensor temperature. Statistical analysis of data obtained from a 100 x 150 imager at room temperature indicates that the minimum pixel rate that can be used at -40°C will be somewhere near 2.5 KHz. This prediction is based on a minimum amount of data, and will have to be corroborated by further experimental work before a great deal of confidence can be placed in it.

Another effect which might be expected to limit the minimum output data rate, at least in surface-channel CCD imagers, is low-frequency degradation of charge transfer efficiency produced by trapping of carriers in oxide traps. It has been theoretically predicted* that the CTE will begin to fall, because of oxide traps, at frequencies below about 1 KHz. However, as will be discussed in Section V., experimental work at TI with surface-channel CCD's has shown no evidence of reduced CTE at low frequencies, even down to 100 Hz. In a 400 x 400 area array, operated at 10^4 pixels per second output rate, the clock rate in the parallel imaging registers will be 25 pixels per second, so there remains the possibility of reduced parallel register CTE at such a low output data rate. Further experimental investigation of the CTE at very low frequencies is called for to resolve this question.

L. Blooming

While several companies have reported some success in controlling blooming in CCD imagers, the techniques require additional fabricational complexity and reduce the effective sensitivity of the imager at normal and low light levels as well as at high light levels. As a result of the increased complexity of device processing, it is expected that a considerable yield loss would be experienced in an anti-blooming design, particularly in large arrays. Thus it is felt, in the present application which calls for a replacement of the silicon vidicon having smaller size, weight, and power consumption, but not necessarily higher anti-blooming performance, that this feature is a luxury not worth its cost. Thus, the imager is predicted to bloom when a pixel becomes saturated. However, given the large dynamic range of the CCD sensor, it is anticipated that there will be few occasions when the intrascene contrast will be high enough to necessitate saturation of a pixel, and hence blooming should present no undue limitation to the performance of the sensor.

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*R. D. Melen and J. D. Meindl, "A Transparent–Electrode CCD Image Sensor," presented at the 1973 IEEE Solid State Circuits Conference, Philadelphia, February 15, 1973.

M. Environmental And Life Tests

The following specifications should be considered at the present time as only estimates because more experience and experimentation with the devices are needed before acceptance test criteria are firmly established.

1. Operating Temperature

The array shall meet all imaging performance requirements while operating at -40°C. Operation at temperatures between -60°C and +45°C for a continuous period of ten hours shall not cause permanent degradation.

2. Operating Life

The array shall not exhibit any degradation in performance while operating continuously at the recommended temperature and voltages at an input irradiance of two (2) watts m^{-2}, for a period of not less than 2,500 hours.

3. Non-Operating Life

The non-operating life, defined as the time during which power is not applied, shall be in excess of 5 years at any temparature between -40°C and +25°C. The array shall not exhibit any degradation in performance following this duration of accumulated non-operating time.

4. Shock and Vibration

The array shall meet all imaging performance requirements after a non-operating exposure to each of the following environments:

a.   Sinusoidal vibration—vibration in all three axes of one octave per minute at the following levels:

(i)   5 to 30 Hz at 0.75 g rms,

(ii)   30 to 200 Hz at 15 g rms,

(iii)   200 to 1000 Hz at 9 g rms,

(iv)   1000 to 2000 Hz at 6 g rms.

b.   Random vibration- vibration along all three axes for 60 seconds per axis at 18.1 g rms shaped spectra as shown in Figure 3-4.

c.   Mechanical shock—two 250 g, 0.5 ±0.1 ms terminal peak sawtooth shocks along three axes. (12 tests).

5. Radiation

The sensor shall not fail to meet performance specifications after either a cumulative dose of 10^5 rads of ionizing radiation or after dislocation damage equivalent to that induced by a fluence of 10^{11} 1 Mev equivalent n cm^{-2}.

Figure 3-4. Spectrum for Random Vibration Tests

SECTION IV

RATIONALE FOR DESIGN CHOICES

A. Introduction—Confidence Level

Every novel gadget at one time existed only as a concept. In this sense, a particular Area Imager and a particular Linear Imager have been visualized as having certain features that are described in Section II of this report. Inherent within this vision is the fact that the Imagers are to be actual pre-production items at the end of the Development Program. The Imagers are, therefore, restricted in one way to having only those features, dimensions, and numbers of elements that will allow the vision to become a reality and in another way to only those imagers that can meet the design goals as given in the Study Guidelines and in Section III of this report. The choice of a configuration, an electrode and a channel structure, the number of elements, the scanning mode, the specified dimensions, and other features have had to provide a high confidence that these two restrictions will endure; that is, we have had to make choices that will ensure success during the Development Program, assuming of course that sufficient talent and hard work are devoted to the Program. In this Section of the Report, reasons for the various decisions and choices are given.

Probably the most elusive choice was the number of elements in the Area Imager, and for that reason factors related to the number of elements are discussed in greater detail than the others. The considerations involve the fabrication of the device itself and the manufacture of the photomasks. These two factors are discussed in the order named.

When the number of elements in the Area Imager is increased, the overall device area also increases and the device fabrication becomes more complicated in several ways:

1) A raw silicon slice with the same homogeneity over a larger area is required;

2) A larger backside area must be thinned,

3) A larger surface area requires the same flatness tolerance,

4) A larger reticle for making photomasks is required, and

5) The probability of a flaw per unit area occurring on the photomask and also on the fabricated device goes up exponentially with the area.

The overall area can be reduced if dimensions of the MOS structures are reduced, but a 22.9 μm pixel size is already stretching photolithographic tolerances. The probability of a flaw occuring also increases by some factor of the reduction of dimensions. An increase of the overall area above that required for a 400 x 400 array with pixel size of 22.9 μm will soon bring about a change in the method of producing the photomask from single reticle production to reticle composition which is discussed in the second next section following.

B. Sensor Configuration Versus Fabrication Techniques

1. Trends in Packing Density.

It is difficult to predict the maximum number of elements per array — or the maximum packing density of elements on a chip — that will be being produced with reasonable yield in the Fall say of 1975. Some comparisons with integrated circuits may help. As there are with integrated circuits (see *Solid-State Electronics 15*, 819 and 891 (1972)), there may be fundamental limitations based on such factors as power dissipation density, minimum supply voltage, oxide breakdown, substrate doping fluctuations, and metal migration. However, now in the Fall of 1973, and in the near future, the limitations have to do with the technology of fabricating the devices. In the case of integrated circuits, the number of devices per chip doubled approximately every year beginning with the first planar transistor in 1958 and continued to the present time. In spite of the steadily increasing circuit complexity and packing density, yield remained about the same over the years. If we say that a 100 x 150 element CCD image sensor was made in late 1972 and double the number (15,000) elements every year to the fall of 1975, we would have a 300 x 400 array (120,000 elements). By this kind of guessing, our number 160,000 (400 x 400) is at least optimistic. The technology of CCD image sensors benefits by all the knowledge and experience accumulated during the development and production of integrated circuit, especially MOS, devices; and that is one reason why the area imagers are as large (in number of elements per chip) as they are today, although they seem small when compared with what we would like for them to be.

2. Device Fabrication

To get an understanding of the defects that may appear on a newly manufactured CCD chip let us discuss the modifications that are made on the surface of the chip as it goes through its several processing steps. To illustrate the processes, a specific configuration consisting of a 3-phase, overlapping electroce, and buried channel structure has been chosen. Processing steps that are typical but not necessarily the ones that are actually in use are discussed. For the present let us consider a small portion somewhere in the "middle" of the matrix, that is, a region well separated from the input and output circuits and the clock drive *bus lines*. Those processing steps that are required by structures outside the actual 500 x 500 matrix will be ignored. We start with a lightly doped p-type silicon wafer and deposit silicon nitride on its surface. Then using a photoresist and etching process we cut through the nitride and produce lines of p^+ material by diffusion through the openings in the nitride. We can visualize the structure better by referring to Figures 4-1 through 4-6. Figure 4-1 shows a section through the silicon slice perpendicular to the lines. Next the windows are filled in by growing a thick oxide. Finally, the nitride is stripped, a thin oxide is grown (Figure 4-2) and the buried channel implement is made (Figure 4-3).

From a view looking down on the surface that we are considering, if we could see the different types of diffusions, the surface would appear as shown in Figure 4-4 with typical dimensions of the stripes shown. The wide n^+ region forms the buried channel for the vertical lines. the p^+ strips become the channel stops.

Let us change our viewpoint again, this time looking at a section of the silicon parallel to the strips but cut in the middle of the vertical channel. Metal electrodes are formed as follows by a deposition, photoresist, and etching processes. Metal is deposited on the surface and then etched to leave one set of metal electrode stripes perpendicular to the channels. The electrodes are then

Silicon Nitride

P⁺ Diffusion

P⁻ type Silicon
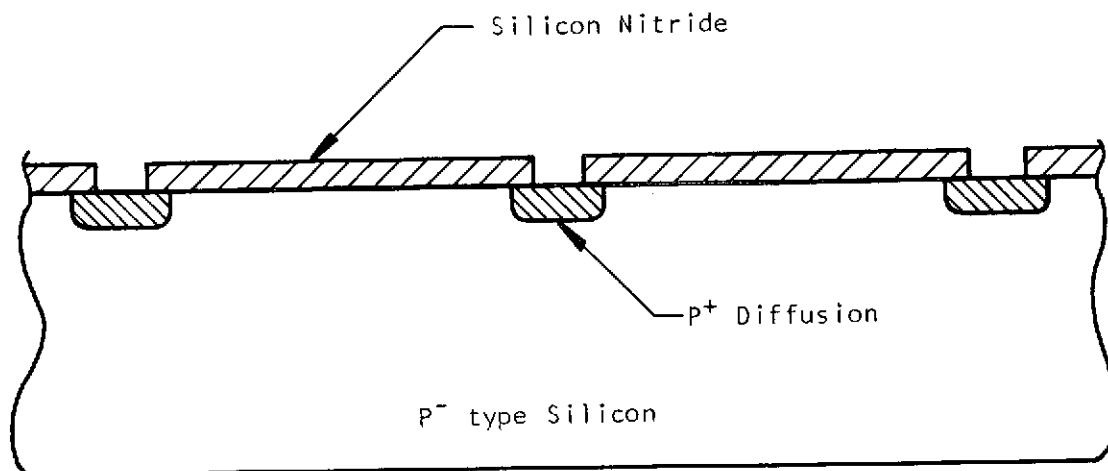
Figure 4-1. Section During Device Processing Illustrating
Channel Stop Diffusion

SILICON DIOXIDE

P—TYPE SILICON
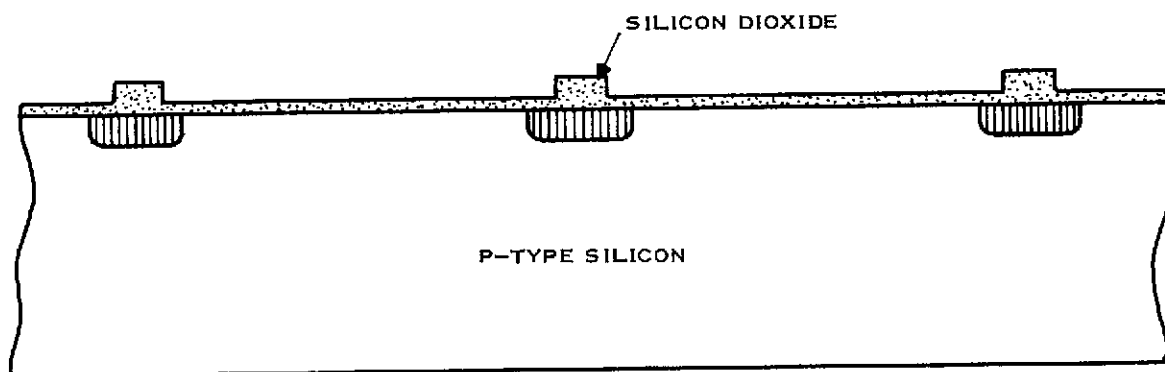
Figure 4-2. Section During Device Processing Illustrating
Thin Oxide Growth

ION IMPLANTED BURIED CHANNEL

P—TYPE SILICON
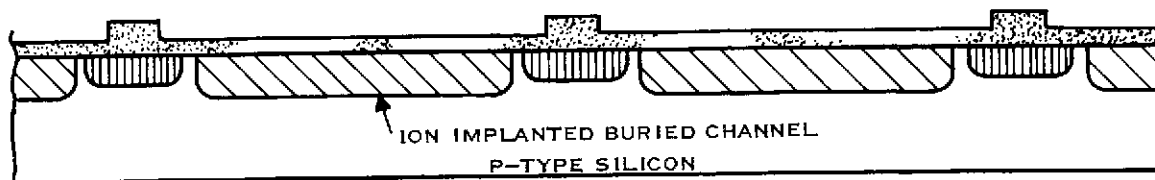
Figure 4-3. Section During Device Processing Illustrating
Channel Ion Implantation

22.9 μm

5.1 μm | 17.8 μm

Vertical Buried
Channel
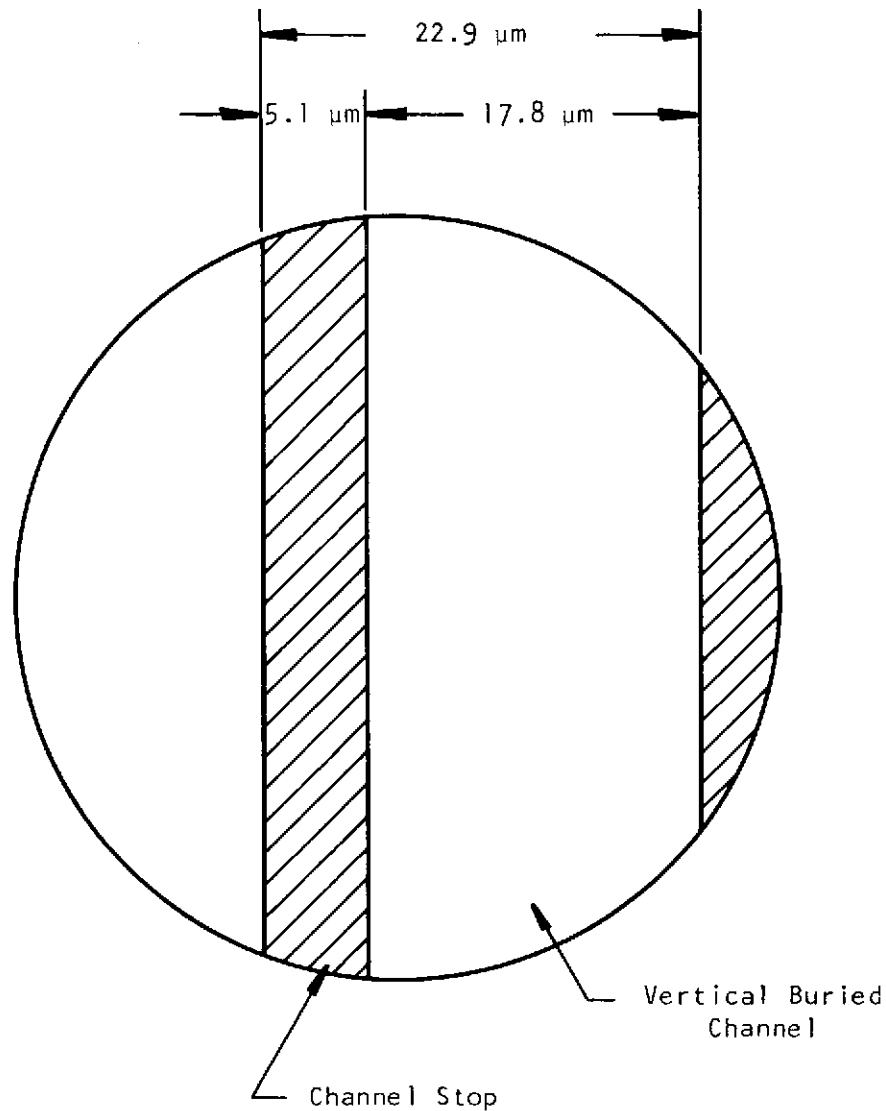
Channel Stop

Figure 4-4. Schematic Showing Channel Stop During Device Processing

anodized to give us the section shown in Figure 4-5. A second layer of metal is deposited and patterned to form the intervening electrodes. Finally, the surface is coated with a protective oxide and the section shown in Figure 4-6 results.

Dimensions shown are typical for those devices made by photolithographic processes. If devices can be made by an electron beam lithographic process, a different, generally smaller, set of dimensions would apply.

In a 500 x 500, physically square device using 3-phase clocking, there are 1500 metal strips each 0.45 inches long with electrode widths of 0.29×10^{-3} inch; there are then about 57 feet altogether of electrode stripes. There are 500 buried channels each 0.45 inch long or almost 19 feet of channels and a channel stop on each side of the channel or about 19 feet of channel stop. If the
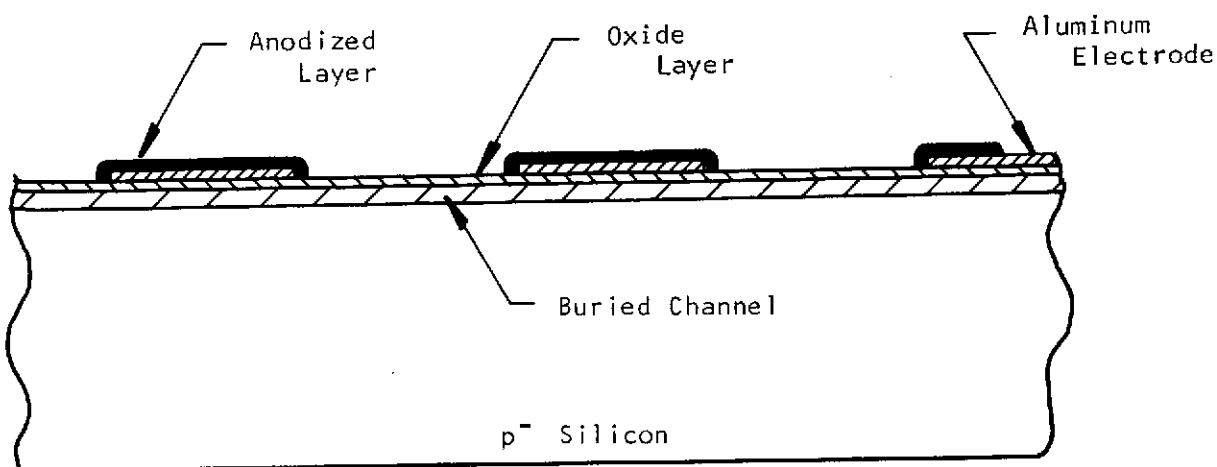
Figure 4-5. Section During Device Processing Illustrating Anodized Electrodes

devices are for a frame store mode of operation these last two mentioned dimensions are doubled. The minute widths, minute separations, and relatively immense total lengths of these parallel, crossing, and overlapping stripes provide many chances for flaws to occur.

3. Kinds of Defects

The intricate metalization pattern is a major source for fatal defects. A short across the electrodes anywhere makes the device worthless. This kind of defect as well as shorts to the substrate, which might be caused by pinholes in the oxide, can be detected in dc tests performed on the uncut wafer. Pinholes through the nitride can allow spots of diffusion that cause severe effects on both the charge transfer efficiency and the dynamic range. It is suspected that the spread in
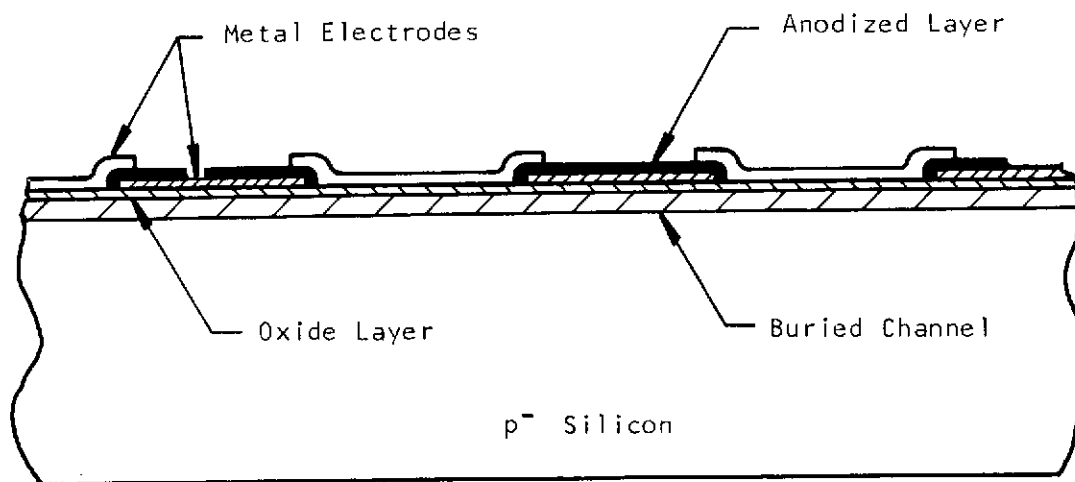
Figure 4-6. Section Illustrating Electrode Structure Over the Buried Channel

transfer efficiency stems mainly from bumps in the surface potential in the transfer gaps, produced by an uncontrolled amount of surface or oxide charge. In single level, non-overlapping electrode devices, the channel oxide is partially exposed thus causing gross alterations of its operating characteristics when ionic contamination (i.e., breathing on the device) reaches its surface.

There is a wide variety of "white" defects, that is, spikes in dark current that can occur. Besides the localized generation centers that produce dark current spikes, there are other white defects that are strongly voltage and/or light sensitive. They seem to be associated with some kind of a breakdown effect, possibly at the boundary of the channel-defining diffusion.

Another kind of defect that is characteristic of charge transfer devices appears in the display as black bars. This is produced by some kind of defect causing a barrier in one of the transfer channels. One possible source of these is a bridge of the channel stop diffusion across the transfer region. Another is a pinhole through the oxide, small enough to cause no detectable shortage, but sufficient to drain out all local charge from the channel.

If the device is operated in a frame transfer mode, both black and white localized defects have an appearance in the display that depends on their location to the device. Individual, extra-signal current sources in the imaging area appear as white spots, whereas they are smeared out when located in the storage area. If a blockage occurs in the imaging area, black bars start at the corresponding location and extend in the vertical direction all the way to the output register. A blockage in the storage area turns a whole column black, and if it happens to be in the serial register it leaves a black field.

C. Electrode and Channel Structure

1. $A\ell$-$A\ell_2 O_3$-$A\ell$ Electrode Structure

A 3-phase overlapping $A\ell$-$A\ell_2 O_3$-$A\ell$ electrode structure (see Figure 2-2) has been recommended for the following main reasons:

1) An overall minimum pixel size is achieved.

2) The 3-phase, single-level structure provides the directionality for the charge transfer, but also reduces the fabrication complexity when compared with 2-phase structures and reduces the number of transfers when compared with a 4-phase structure.

3) The overlapping electrode structure relaxes the photolithographic tolerances during electrode definition, and reduces the electrode separation to the thickness of the anodized layer.

The advantages of the double level, or aluminum-aluminum oxide-aluminum, electrode structure that is proposed derive from the disadvantages associated with other types of electrode structure (see Appendix B). Let us first consider these disadvantages: First, the electrode spacing should be small, 3 micrometers or less, to ensure a sufficiently close potential coupling between electrodes so that the transfer of charge is facilitated. The closer this spacing, the tighter are the dimensional tolerances during the photolithographic processing. The elimination of the close spacing requirement during photolithographic definition of the electrodes is a significant advantage. Second, the exposed layer of oxide between the electrodes causes the device operation to be

sensitive to ambient effects. For example, on an SiO_2 surface exposed to the ambient, ionic charges tend to accumulate and migrate under the influence of the electric fields. These migrating ions cause a mirror charge in the silicon substrate that modify the potential barrier at the Si-SiO_2 interface, thereby causing changes in the operating characteristics. A two level system effectively seals the outside surface from ambient effects.

The proposed electrode structure is a novel double level metallization technique in which both metal levels are aluminum and the insulation between the two metallization metals is aluminum oxide produced by anodization. The anodized technique provides a simple, quick, method for forming the double level system insulation. The insulation thickness of the aluminum oxide forms the interelectrode gap, which allows normal metalization definition tolerances to be used. The double level structure also seals the electrode gap from ambient effects and provides a coplanar, overlapping, high conductivity metallization system. The separation between electrodes in the aluminum-aluminum oxide-aluminum system is the thickness of the anodized layer, a separation so small that the conventional photolithographic processes could not approach it. The narrow gap allows the fringing fields from the electrodes to suppress the potential barrier at the semiconductor surface. The removal of the barrier, in turn, allows a more complete transfer of charge to take place from one electrode to the next. The improved stability of the aluminum-aluminum oxide-aluminum system over the single level aluminum system is explained by the sealed condition of the silicon oxide surface between electrodes. The silicon dioxide surface between the electrodes in the double level system is covered with a layer of aluminum oxide which is covered with a layer of aluminum. Thus, surface migration of charged ions on the SiO_2 surface is prevented.

Since the anodic oxide is grown atomistically on the metal itself, the adhesion between the metal and its oxide is excellent. It is also noteworthy that all surfaces exposed to the anodization condition, regardless of their topology or geometric orientation, are coated uniformily, since the propagation of the oxide metal interface is perpendicular to the applied electric field. In addition, anodic processes are inherently self-healing, as the maximum rate of conversion is found at the points of maximum field across the oxide film so that the thinest oxide areas and pinholes in the oxide film are self-eliminating. The thin gate oxides exposed to the electrolyte and the applied field encountered in the anodic portion of the fabrication process are not affected if care is exercised in the selection of the electrolyte and externally applied potentials.

Aluminum oxide is recognized as a dielectric, and the electric properties of the anodic form are well referenced. Results indicate that the anodic oxide of aluminum has a resistivity in excess of 10^{16} ohm-cm and a dielectric constant of approximately 8.6, with very little frequency dependence. Anodized films ranging from 700 to 6000 Å are routinely grown in the fabrication of CCD's, and the breakdown strength of the films exceeds 6×10^6 V/cm. The pinhole density is less than 3 cm^{-2} with a 5000 Å thickness of aluminum oxide.

The process steps used to fabricate a CCD using the aluminum-aluminum oxide-aluminum double-level metallization system are summarized in Figure 4-7:

Figure 4-7a — After the thick oxide is formed, the source-drain diffusion is made and the thin gate oxide has been grown, a layer of aluminum is evaporated over the entire wafer.

Figure 4-7b — The aluminum is then patterned to form the first-level electrodes.

Figure 4-7C — Patterning may be performed using standard photolithographic techniques so that the minimum length of the electrodes may be 7.4 μm (0.29 mil), and the separation between electrodes on the same level may be 5.1 μm (0.2 mil) or greater. Next, selected portions of the aluminum are covered with photoresist; these portions include via holes from the first- to second-level metal for bond pads and the anodizing connections. In a double-level metallization system, there is no need for the clock electrodes to contact the semiconductor substrate; however, the electrochemical anodization process requires electrical connection to the anodizing contact. Typically, this anodizing contact (bus) is an extension of the first-level metal which is run to the scribe line. The first-level metal is then anodized; the portions covered with photoresist remain un-anodized.

Figure 4-7d — The anodizing converts an outer layer of the aluminum electrodes to $A\ell_2 O_3$.

Figure 4-7e — The protecting photoresist is then stripped and the second layer of aluminum is evaporated over the entire wafer.
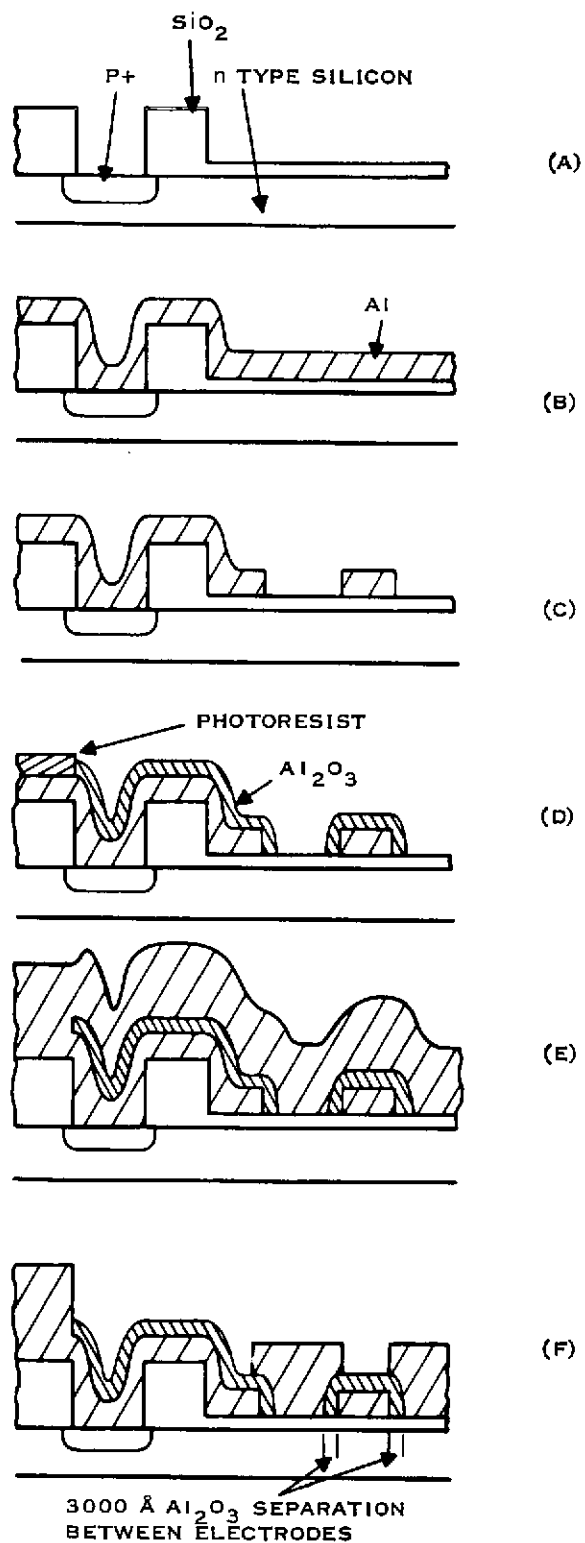
Figure 4-7. Process Steps in the $A\ell\text{-}A\ell_2 O_3\text{-}A\ell$ Electrode Structure Fabrication

Figure 4-7f — The second level of aluminum is then patterned, using standard photolithographic methods and acidic subtractive etching. The patterning is performed so as to interleave the second-level CCD electrodes between the first-level CCD electrodes.

The resulting structure consists of a set of coplanar but overlapping electrodes separated by a layer of anodized aluminum. During the patterning of the second metal level, the anodizing contact (bus) to the first-level metal is also removed. The entire fabrication process can be accomplished with only one more photomask (the second-level metal photomask) than is used to fabricate a single-level metal CCD. A reversal of the photomask normally used to open the protective oxide overcoat in the bond pad areas may be used to protect portions of the first-level metal from anodizing.

2.   Buried Channel Structure

The surface channel, charge-coupled device, as described in Appendix A, operates by moving minority carriers along the interface between a semiconductor and a dielectric layer with the application of voltage pulses to metal electrodes, the electrodes being insulated from the semiconductor by the dielectric. The characteristics of the transfer along the interface from the region near one electrode to a region near the next is determined by the minority carrier transport under the influence of their own potential, fringing fields, and diffusion, and by the trapping properties of interface states. (See the sections on surface states and charge transfer inefficiency in Appendix A.) Certain limitations are inherent in the transfer of charge along the interface, for example, a reduced charge transfer efficiency and an increase of noise. The limitations are such as to require the introduction electrically of a uniform "fat zero" into the array of wells before each exposure to light. These limitations may be appreciably reduced by the use of a buried channel structure, which is described in the following paragraphs. An energy-band diagram is shown in Figure 4-8.

In buried channel devices, minority carriers are confined to a channel that lies beneath the surface of the semiconductor. The buried channel is created by an n-type diffusion or ion implantation into the p-type silicon. Bulk trapping of charges should be several orders of magnitude less important as a charge loss mechanism than surface state trapping. The introduction of a large fat zero should no longer be required. Certainly the quantity of electrically introduced background charge needed is significantly reduced, and the designation "slim zero" would apply. Because of the increased fringing field under the electrodes, diffusion is replaced as an important factor in the intrinsic transfer process by the more powerful field-aided transfer. Mobility of minority carriers is higher in the bulk than at the surface. Hence, the transfer of charge should be faster and more efficient.

One potential disadvantage of the buried channel is that since the charge is stored across a thickness of depleted silicon as well as the oxide, the effective capacitance is decreased and the charge-handling capability is less than that for comparable surface channel devices. However, fast interface state noise is no longer present, so the noise level of the buried channel CCD will be considerably smaller than that of the surface channel device.

An advantage is inadvertently realized by a combination of the overlapping, $A\ell$-$A\ell_2O_3$-$A\ell$ electrode structure described in the preceding sub-section and the buried channel structure. One of the major factors causing the buried channel device to differ from the surface channel device is
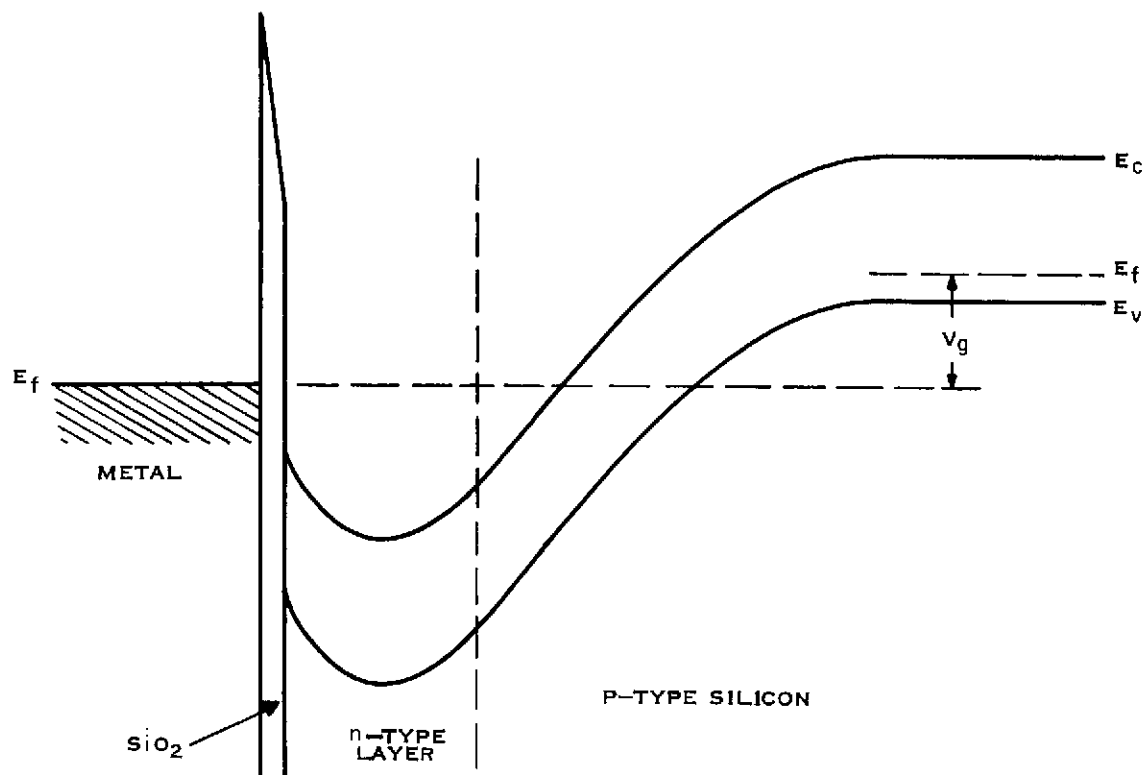
Figure 4-8. Energy Band Diagram for a Buried Channel on a P-Type Silicon Substrate

illustrated by the relationship of the gate-oxide capacitance to the depth of the potential well produced by that gate (ref. 44). Given two identical gate electrodes at the same potential, in a surface channel device the gate with the larger oxide capacitance will produce the deeper well at the interface. In a buried channel device, the gate with the smaller oxide capacitance will produce the deeper well in the depleted channel. This argument may be used to show that the effect of a gap between adjacent electrodes is quite different for a buried channel than for a surface channel device. In a buried channel CCD, the effective channel capacitance under the gaps is very small, and very deep potential wells result. These undesirable potential wells, which are discussed in a later paragraph, in buried channel devices tend to interfere with the potential wells under the gate electrodes, which consequently cannot properly control the storage and transfer of charge. Better control of the interelectrode gaps can be achieved by the overlapping electrode structure because the gaps between electrodes are reduced to the thickness of the anodized layer.

The buried channel structure is illustrated in Figure 4-9 as a 3-phase, p-channel CCD (ref. 68). It consists of a p-type layer of Si on an n-type Si substrate with p^+ contacts at either end of the channel. The structure is completed with an SiO_2 film and metal electrodes. The thickness of the p-layer is a few μm and the acceptor concentration is 10-20 times the donor density of the substrate. In order to form a buried channel, it is necessary to deplete completely the p-type layer and part of the adjacent n-region. This is accomplished by putting the output diode at a voltage V_0, a reverse bias strong enough to drain all of the holes out of the p-layer (a total charge of the order of 10^{12} cm^{-2}. A solution of the one-dimensional Poisson's equation for this depleted condition is shown in Figure 4-10, where it was assumed that the p-layer has a uniform concentration of $2 \times 10^{15} \text{ cm}^{-3}$ and is 5 μm thick, and the SiO_2 is 1000 Å thick. The substrate is taken to be uniformly
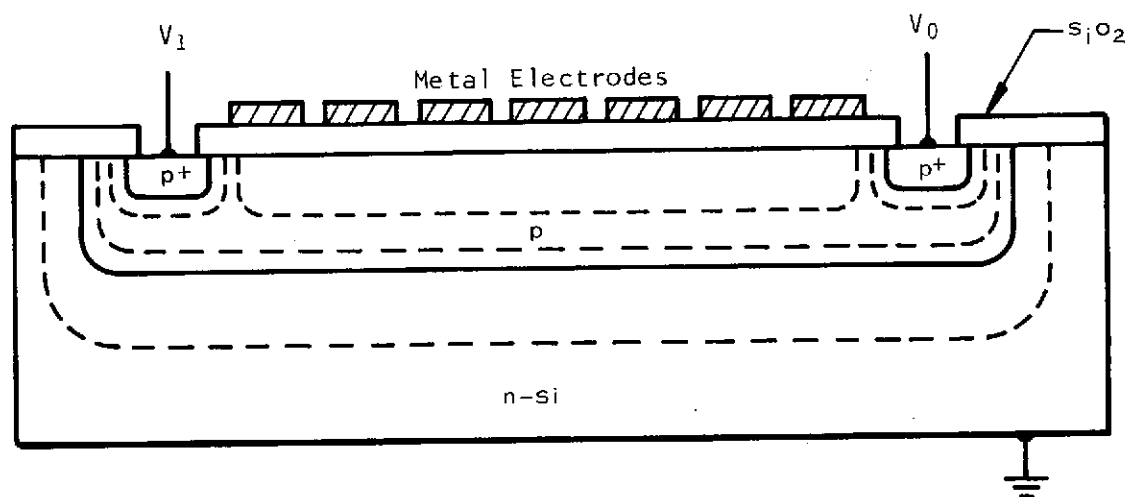
Figure 4-9. Cross Sectional View Illustrating the Construction of the Buried Channel (Reference 68)

doped to 1×10^{14} cm^{-3}. The graph shows positive potential plotted upward as a function of distance away from the Si-SiO$_2$ interface for an applied gate voltage of 0 V. One peak at -37V in the curve represents a potential minimum for holes, and its position, about 4 μm from the interface, is the buried channel. This value of peak voltage also gives some idea of the potential that must be applied to the output diode in order to deplete the p-layer.

The charge-carrying capability of this structure has been estimated to be about 4×10^{-8} C/cm^2 and the effect of this charge on the potential is shown in Figure 4-10. A surface device
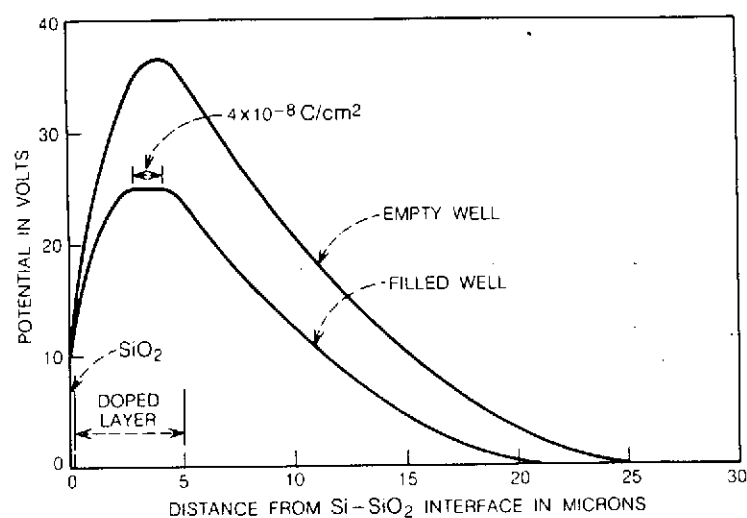
Figure 4-10. Potential as a Function of Distance into Silicon from the Interface for an Empty and a Full Well (Reference 68)

would accommodate a charge load of about 3×10^{-7} C/cm^2, almost an order of magnitude more, and this is one of the penalties of using a buried channel structure, a reduced charge capacity.

In order to ascertain the fringing fields in the channel, two-dimensional potential calculations have been made (Reference 68) numerically using the buried channel structure. The first structure considered for this calculation, corresponding to an experimental device, is shown in Figure 4-11 and consisted of 45-μm-wide plates with 5-μm interelectrode gaps. The channel potential curve in Figure 4-11 shows a rather disturbing feature, i.e., the existence of potential wells under the interelectrode spaces. It is understandable that such wells will exist since the floating region between the plates would go to -800V without the influence of fringing fields from the grounded plates. These wells will, of course, fill with mobile charge, but the amount contained in each is going to depend on the potentials of the spaces under the neighboring CCD plates. This means that the wells can exchange charge with any signal that might be present, leading to a severe loss. It would be desirable then to have the interelectrode potential vary monotonically across the gap; one way to do this would be to let the spacing go to zero. The potential calculation was repeated for the configuration shown in Figure 4-12 for a plate length of 10 μm and for a zero spacing between metals. Two curves are shown, one for the buried channel CCD and one for a surface device for comparison. Here, the undesirable charge pockets are clearly missing and there is a significant amount of tilt in the potential under the plate at -10 V (the one where charge would be transferred from). The surface device, on the other hand, shows a relatively flat potential. The field under the -10 V plate for the buried channel is at least 3×10^3 V/cm, while the minimum field for the surface device is about 10 times smaller. Transport calculations, using this field value and the indicated plate length, show that only 10^{-7} of the charge will remain behind after 1 ns. Thus operation of the shift register at a clock frequency of several hundred MHz should be possible.
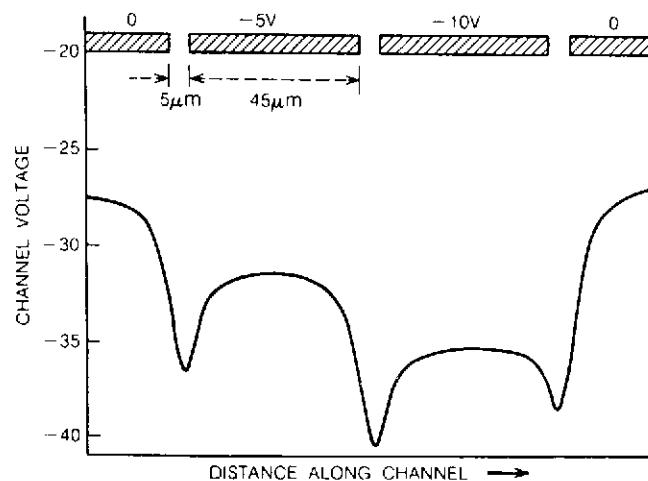
Figure 4-11. Two-Dimensional Plot of Calculated Potential along the Buried Channel and Finite Electrode Separation (Reference 68)
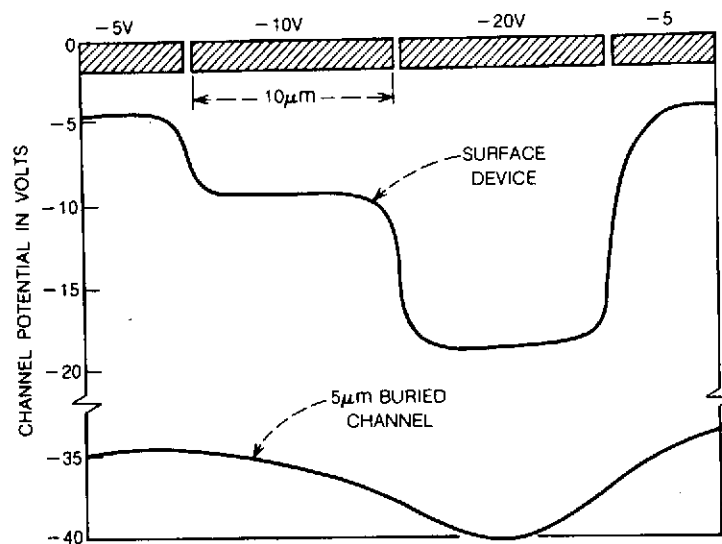
Figure 4-12. Two-Dimensional Plot of Calculated Potential Along a Buried Channel and Along a Surface Channel for Zero Electrode Separation (Reference 68)

D. Array Size — Photomask Production

In this section of the report it will be shown that, for arrays larger than approximately 400 x 400 elements, photomasks will have to be made either by reticle composition or by electron beam lithography. An explanation of what reticle composition is, why the method will be required, and why the method is particularly formidable for CCD arrays is given. To establish a viewpoint we start with a brief description of photomask and reticle production.

One photomask is required each time, during the fabrication of the devices, that a layer of photoresist has to be deposited on the chip, then exposed, developed, and the portion that remains soluble washed away. Then wherever the resist remains, the surface will be protected when the exposed areas are treated by such processes as etching away a layer of oxide or metal that had been previously grown or vapor deposited, respectively, over the entire surface. The oxide or metal in these latter cases is said to be patterned.

A photomask generally contains multiple images of the pattern that is being processed. Hence, for example, if the photomask contains 15 images, 15 devices on a single slice of silicon are being processed at the same time. The multiple images are formed on the photomask by photographic processes the first of which is exposing the plate with a combination step and repeat and reduction camera. The plate used for the object in this step and repeat-reduction process is the reticle. The cameras used in the reduction process are highly specialized optical systems providing extremely fine image definition. As with all specialized optical systems, they cannot be used except for their specified applications without appreciable sacrifice in optical image quality. The largest reduction ratio that can be used is 1/5. The photomask stage is driven by a programmable computer and provides 2-dimensional platform translation with extremely high positioning precision. The reticle itself is made in a machine called a pattern generator, somewhat like an enlarger with an adjustable aperture in place of a photographic transparency.

In the manufacture of integrated circuits, MOS devices, and CCD's, certain design rules are established for such things as minimum widths of metal strips and separation between metal electrodes, maximum electrode lengths, minimum widths of clock bus lines, and the amount of overlap in double level construction. These design rules are established on the basis of electrical requirements, attainable optical resolution, the chances that flaws — shorts and open circuits — may occur, allowances for lateral diffusion, etching, and undercutting of resists, and the precision with which a photomask can be aligned with structures that have already been placed on the slice.

When we begin with the minimum dimensions established by these design rules and go back through the 1/5 reduction to a reticle size that can be accomodated by the step and repeat cameras, we find that the maximum size of an image made from a single reticle is limited. As was pointed out in a preceeding discussion, the largest size for one of the images, on the photomask, that can be produced from a single reticle is 0.49 by 0.49 inch.

Whenever a completed device is so large that a given pattern, for one of its processing steps, cannot be placed on a single reticle, a process known as reticle composition can sometimes be resorted to. Reticle composition is illustrated in Figure 4-13 which shows schematically, for example, a portion of the upper right hand corner of a pattern related to the active area for a device that was exposed on the photomask while using a first reticle. Space was not available on the first reticle to include the bonding pads. Consequently, a pattern for a bonding pad and its lead were placed on a second reticle. The first reticle was removed and replaced with the second; then the photomask stage was translated until the "impression" of the bonding pad lead made while using the first reticle lined up with the image of the lead on the second reticle. Finally, the bonding pad and lead are exposed on the photomask. As long as the patterns to be aligned are relatively large as the bonding pad leads are, alignment of the second reticle is not particularly difficult.

The size of the matrix area for a 400 x 400-element Area Imager with a pixel size of 22.9 μm by 22.9 μm (0.9 mil by 0.9 mil) is 0.36 inch by 0.36 inch. It has already been explained in a preceeding section that the space between the matrix and the maximum single-reticle area of 0.49 inch by 0.49 inch allows for the serial read-out register, the clock drive lines and interconnections to electrodes, the precharge amplifier, and if necessary, the circuits for inserting a slim zero. Because thinning and special mounting requirements require the bonding pads to be placed somewhat remote from the matrix area, there is just enough room for bond pads within the 0.49" by 0.49" chip area.

Whenever the number of elements is increased from 400 x 400 to, for example, 500 x 500, the size of the matrix of pixels is so large, 0.45 inch by 0.45 inch, that some of the device pattern must be moved from the first to other reticles. An examination of Figure 2-1 shows that at least four reticles would be required. The upper left hand corner could be made the mirror image of the upper right hand corner, but neither could be like the lower left or lower right, which are also different from each other. Unfortunately, although turning a reticle over would produce a mirror image, it would also place the emulsion on the far side of the plate with respect to the lens and an unacceptable degradation of the image would result.

An example, showing why reticle composition to produce photomasks for CCD's will be extremely difficult can be explained while referring to Figure 4-14. The explanation also clarifies why photomask production and device manufacture for 500 x 500-element arrays are development phases beyond the development of 400 x 400-element devices. The figure shows, schematically, composition by using 4 reticles at (a), and an enlargement of a portion of overlapping reticles 2 and
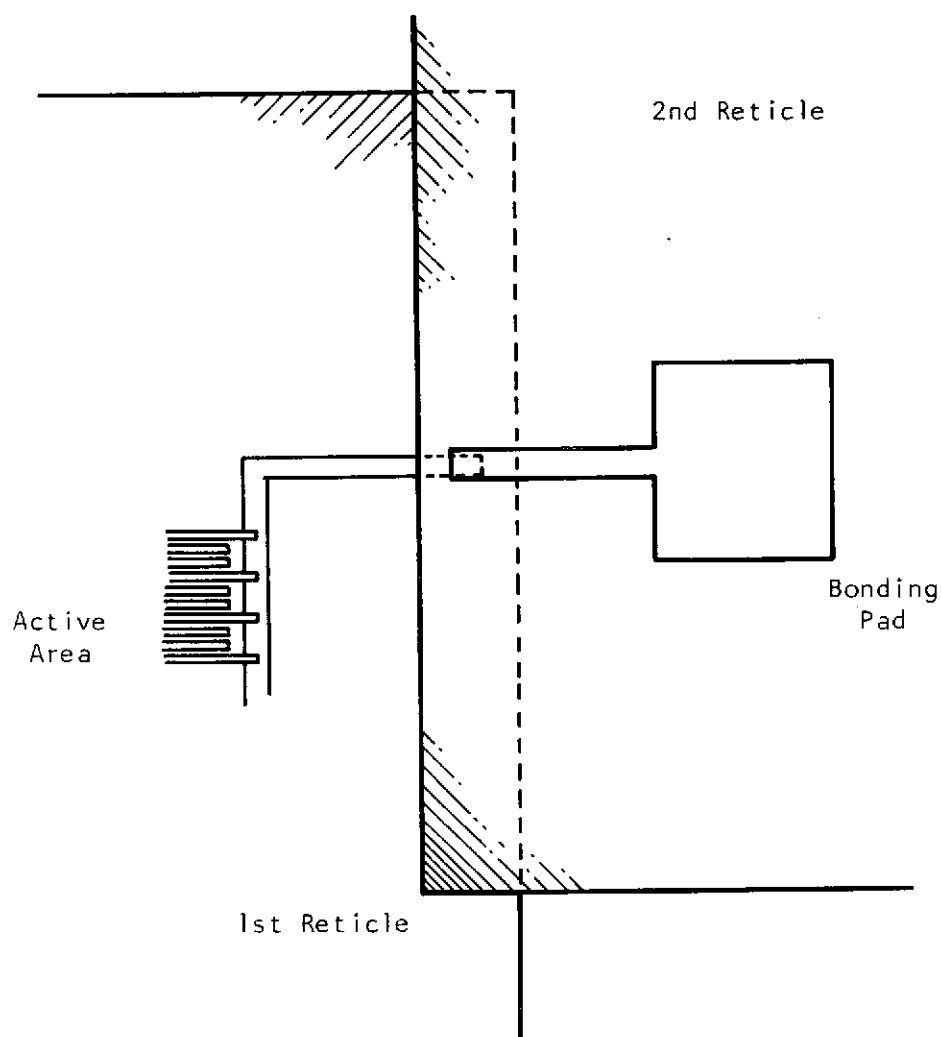
Figure 4-13. Placing Bonding Pad Pattern on Photomask by Reticle Composition

3 at (b), and at (c) a still greater enlargement showing abutted structures (at x) and juxtaposed lines (at y). Widths of lines (or structures) may be as small as the electrode width, 7.4 μm, or the channel stop width 5.1 μm. Too wide a spacing between the juxtaposed lines (as at y) would cause an obvious distortion in an image. An offset of an abutting structure, as at x, is a potential cause of a flaw on the finished device. Two reticles can be aligned with the necessary precision; in fact, linear arrays have been made by using reticle composition. However, the geometry-matching constraints are less severe for linear arrays than for area arrays. For the Area Imager, when the photomask exposure process reaches the fourth reticle, the errors from three previous alignments will have been accumulated; and the alignment is now simultaneously to two reticles (the first and third).
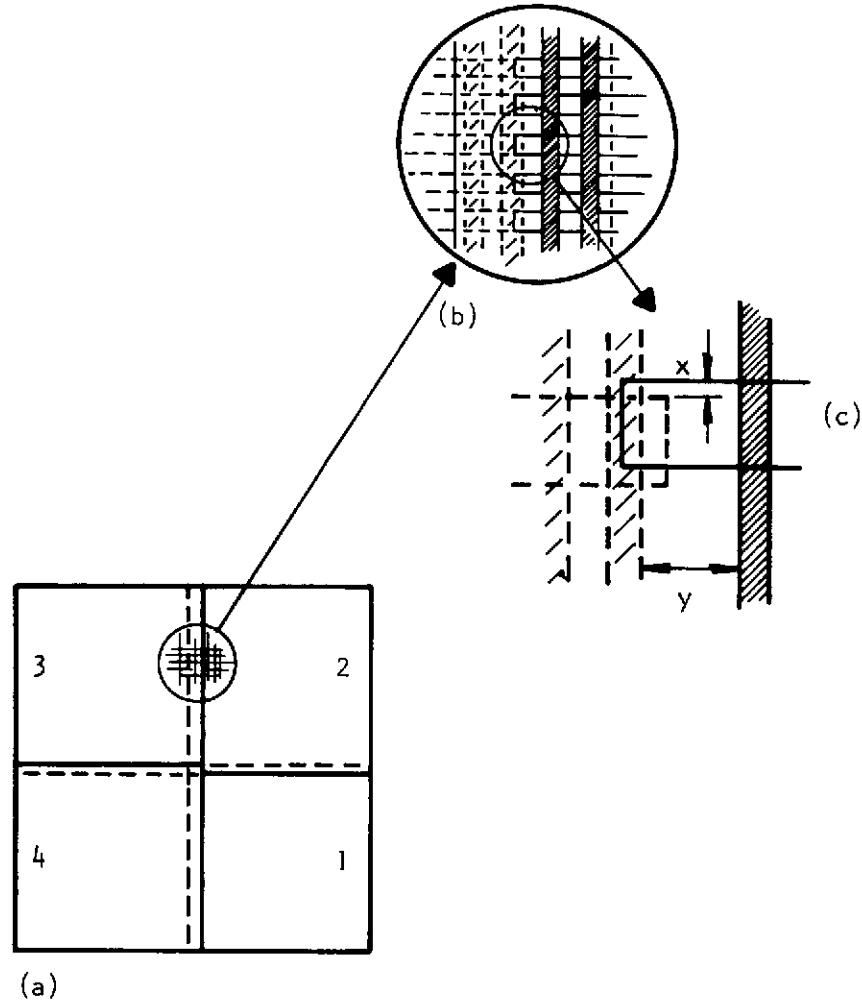
Figure 4-14. Enlargements Showing Abutted and Juxtaposed Lines Illustrating Precision
of Alignment During Reticle Composition

E.   Thinning — Image Plane Flatness

The requirement to thin the Imagers is a consequence of the decision to use backside illumination. Hence, the discussion of thinning and image plane flatness appropriately begins with the relative merits of front and backside illumination.

The overlapping electrode structure recommended in Section II.C leaves the front surface opaque so that front side illumination is precluded. One might consider using some type of transparent electrode—one such is the doped polysilicon electrode discussed in Appendix B—or a structure that leaves a "window" at each pixel; but any of these is only a complication that would certainly have an adverse effect on yield during fabrication of the devices. Also, a window smaller

than a pixel size would affect the spatial frequency response by increasing aliasing as discussed in Section IV. G.1.

When a device having a thick substrate is illuminated on the backside, electrical charges are generated relatively far from the depletion layer. There could be a consequent "crosstalk" between adjacent pixels caused by lateral diffusion of generated charges. Because of the longer diffusion time, there could also be recombination of charges before the minority carriers reach the depletion layer. Substrate thinning is the solution to both of these problems.

Texas Instruments has successfully thinned devices to thicknesses from 10 to 12 μm and has operated thinned devices by illuminating them on the backside, thereby demonstrating the feasibility of thinning and backside illumination. However, additional experimentation needs to be done particularly with respect to thinning larger areas, keeping the image plane flat, and mounting thinned devices.

As pointed out in Section IV. 3., an untreated silicon surface reflects approximately one-third of the incident light energy. A properly treated surface for antireflection can rreduce reflectance so well that almost 1-1/2 to 1 gain in sensitivity is achieved. Once electrons are inside the silicon surface, the internal quantum efficiency, electrons per photons, is almost unity. The gain in sensitivity by antireflection coating is significant. Also, the backside provides a much greater opportunity for coating than the front side.

F.   Antireflection Coating

When light is incident on an optical material, a portion is always reflected, the portion being high for materials having a high refractive index. The reflectance of a polished silicon surface is approximately 35 percent in the wavelength range from 0.4 to 1.2 μm. Consequently, about one out of every three incident photons is reflected and can never be detected by any sensing process that takes place below the surface. Texas Instruments applies a thin-film antireflection coating (ARC) to many of its silicon products to increase the photon absorption. On one light sensor, the reflectance is reduced over a broad range, from 35 to 2 percent at 0.5 μm, the wavelength of minimum reflectance after coating, and to 8 percent and 7 percent at 0.7 μm and 0.4 μm, respectively, by using a 1/4-λ coating of SiO.

Equations for the reflectance of an absorbing medium such as silicon coated with a thin layer of a nonabsorbing (dielectric) material are given in several books (for example, A Vasicek, *Optics of Thin Films*, North-Holland Publishing Company, Amsterdam, 1960, Chapter V). Application of the formulas requires a knowledge of the complex index of refraction, n, of the absorbing medium,

$$\hat{n} = N (1 - ik)$$

as well as the refractive index of the dielectric material. The optical constants, n and nk, as given in the equation, are known as the Drude constants and also as the refractive index and the absorption coefficient, respectively. The constants are usually tabulated with physical constants for materials and usually apply for normal incidence of the light. The constants do depend somewhat on the angle of incidence; consequently, computations for oblique incidence are quite complicated, especially if there is a combination of normal and oblique incidence, as for a diverging or converging beam. Only normal incidence is considered here.

The Drude constants are wavelength-dependent and, in the 0.4- to 1.2-μm range, increase with decreasing wavelengths in silicon. AT 0.6328 μm, n is equal to 3.86 and nk is equal to 0.02.

To find the wavelength at which the reflectance should be minimized, the wavelength is determined where the combination of relative spectral response for the sensor and the relative spectral radiance of the source is a maximum. The composite (or product) curve is found by multiplying the two spectral functions, ordinate by ordinate, at each wavelength as shown in Figure 4-15. The relative spectral radiance for a blackbody at 2,854 K was used, and the relative spectral responsivity shown is for an uncoated Texas Instruments Tivicon*. The composite curve peaks near 0.85 μm. If a 2000 K blackbody had been used, the peak would be at a slightly higher wavelength but still near 0.85 μm. Hence, the reflectance for this combination of sensor and target should be minimized at 0.85 μm.

The curves of Figure 4-15 show that the response at longer wavelengths should be improved if possible, without reducing the overall sensitivity. The 2,854 K blackbody was used because at very low light levels, for example, in overcast starlight, light has a spectral distribution approximately the same as that of a blackbody in the temperature range from 2,000 K to 3,000 K. The reflectance of the coating can be adjusted easily to a minimum reflectance at a slightly longer wavelength.

Figure 4-16 is a plot of the reflectance from a silicon surface as a function of a parameter, x, defined by

$$x \equiv 4\pi \, n_1 \, d/\lambda$$
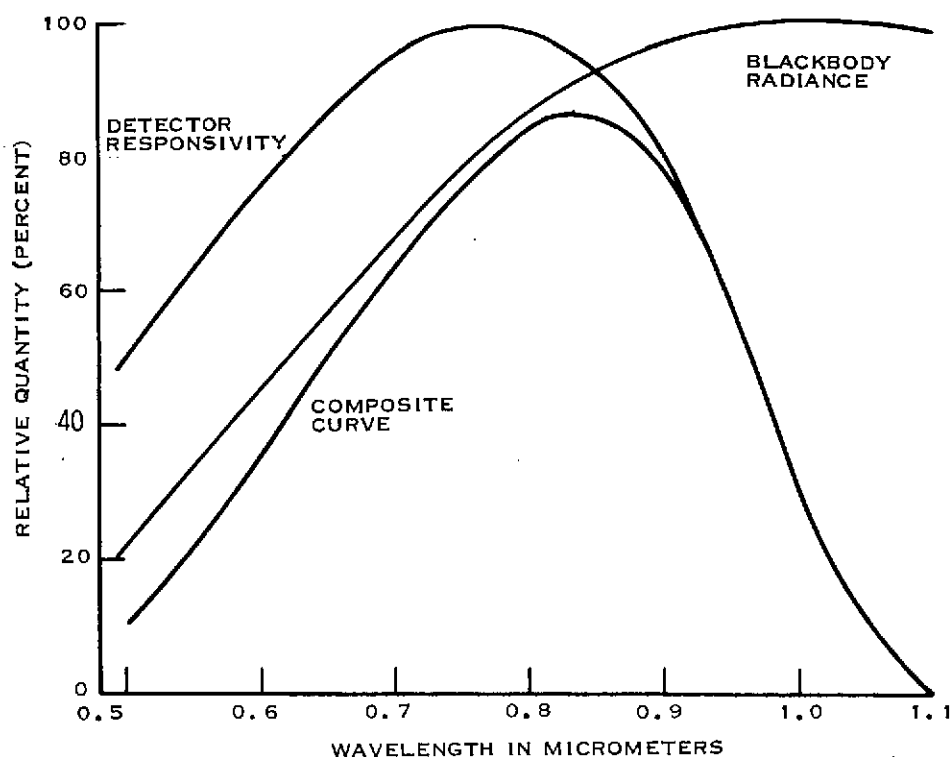
Figure 4-15. Relative Spectral Responsivity of an Uncoated Texas Instruments TIVICON,
Relative Spectral Radiance of a Blackbody at 2854K,
and the Composite, or Product Curve
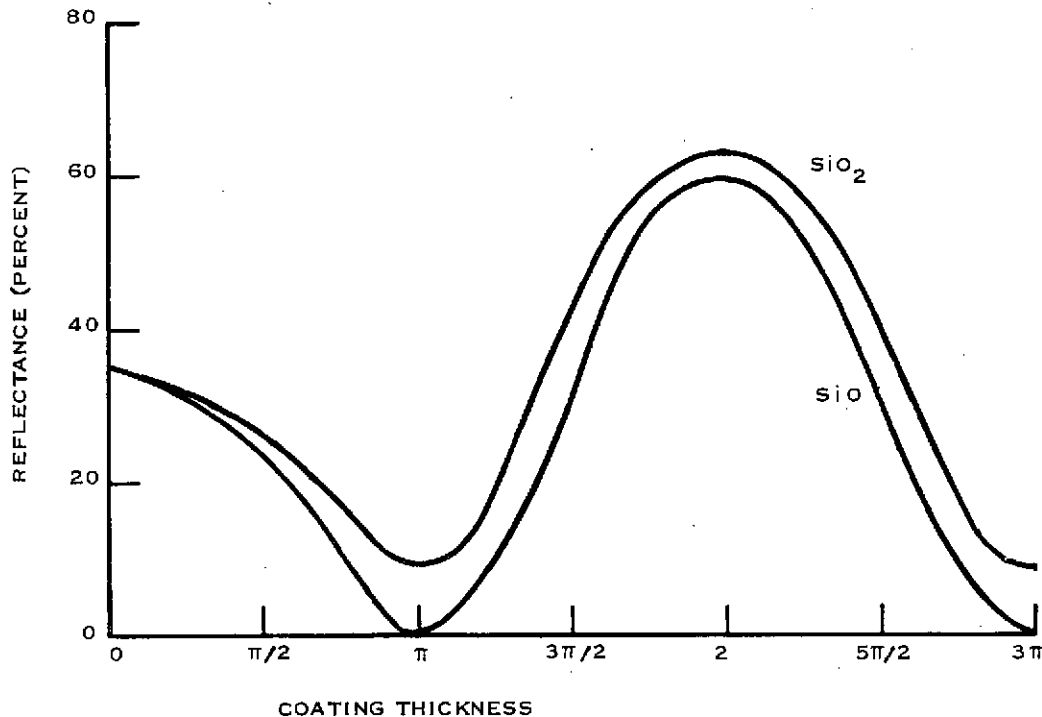
Figure 4-16. Reflectance of a Coated Silicon Surface for Two-Coating Materials (SiO_2 and SiO)
as a Function of the Parameter $x = 4\pi n_1 d/\lambda$

for two coating materials, SiO and SiO_2. In Equation (13), n_1 is the index of refraction of the coating material, d is the film thickness, and λ is the wavelength. For reasons that are not given here, an optimum refractive index for the coating material would be the geometric mean between the index of air and the index of silicon, that is,

$$n_1 = \sqrt{3.86 \times 1} = 1.96$$

Silicon monoxide, SiO, has a refractive index near 1.9 and silicon diode, SiO_2, an index near 1.45. The higher index material is better, and the reflectance at minimum reflectance for the SiO coating is approximately 0.1 of 1 percent.

Figure 4-16 shows that the parameter, x, should be carefully controlled. Since the wavelength has to vary over a wavelength band, d must be controlled to keep x equal to π at the wavelength where reflectance is intended to be minimized. Then, if the thickness doubles, or if the wavelength reduces by a half, the reflectance for the SiO coating can increase to nearly 59 percent. Whenever the reflectance must be reduced more uniformly and over a broader range of Wavelengths, a multilayer coating can be used.

The conclusion that can be made from the above discussion is (1) that the reflectance can be reduced significantly and (2) that backside illumination of the CCD will provide a much better opportunity for antireflection coating. The "structure" composed of the gate oxide plus any overcoating material, normally on the front side, makes the control of both film thickness and thickness uniformity difficult.

G. Operational Considerations

1. MTF and Aliasing.

The proposed sensor pixel size of 0.9 mils square will result in an aperture MTF of 0.69 at 20 lp/mm spatial frequency, as discussed in Section III.A., provided the aperture is an ideal square with an ideal rectangular sensitivity curve (response versus position across the pixel). As explained in Section III.A., the buried channel design will minimize further reduction in MTF caused by charge transfer inefficiency. Thus, with an ideal rectangular sensitivity profile at each pixel, the combined aperture and CTE MTF should be about 0.60 at 20 lp/mm. Because of lateral diffusion of carriers generated in the silicon substrate, the aperture MTF will actually be less than 0.69 at 20 lp/mm, by a factor we may call the diffusion MTF. This factor has been computed for the proposed sensor design, and amounts to about 80%-85% at 20 lp/mm. Thus, the overall sensor MTF should be about 0.50 at 20 lp/mm.

This value is a fairly good compromise between the two competing desirable attributes of unity MTF and no aliasing. Somewhat higher MTF at 20 lp/mm could be realized, and aliasing reduced as well, by making the pixel spacing smaller. However, present CCD processing technology limits the viability of this approach. For a large array, the device yield would suffer considerably using the present technology were the pixel size reduced below 0.9 mil square. If the aperture size were artificially reduced below the pixel center-to center spacing, for example by masking with an additional metal level, to enhance the aperture MTF, the resulting increase in aliasing would probably be unsatisfactory in a number of viewing circumstances.

The sensor is envisioned as being operated in the non-interlaced, full-frame mode. This means that the Nyquist limit frequency will be the same in the vertical and horizontal directions (namely, 21.9 lp/mm).

2. Noise

The reduction of sensor noise was an important consideration in two aspects of the proposed sensor design: the buried channel structure and the on-chip precharge amplifier. Fast interface state noise in a surface channel sensor of the same geometry as the proposed sensor, with a fast interface state density of 10^{10} eV^{-1} cm^{-2}, would have a maximum rms number of fast interface state noise electrons of about 950 electrons per pixel when cooled to -40°C. Although fast interface state noise is highly correlated, and thus will not appreciably interfere with the resolution of lower spatial frequency scenes, it will be significant at frequencies near the Nyquist limit. Since the MTF is rolling off at these higher frequencies, the sensor signal-to-noise ratio would be significantly degraded at high spatial frequencies in a surface channel imager as large as the proposed design.

The on-chip precharge amplifier included in the design for the proposed sensor has been shown experimentally to be a very low noise technique for extracting signal charge from the CCD. Theoretically, a precharge amplifier with a preset node capacitance of 0.07 pF should contribute only about 75 rms noise electrons to the output video signal when cooled to 40°C.

3. Responsivity

The goal of high responsivity was one of the prime considerations in the decision to backside-illuminate the sensor. As mentioned in Section III.H., a frontside-illuminated sensor fabricated at TI had a responsivity to 2854 K radiation of only about 8.7 x 10^{-3} A/W, because of

the screening effects of metal electrodes and insulator layers. On the other hand, a backside--illuminated sensor can be fabricated to have a responsivity essentially equal to that of the TI Tivicon silicon diode array vidicon, which is about 0.1 A/W, a factor of 11.5 improvement.

4.   Fixed Pattern Interference

Fixed pattern interference in CCD imagers can arise from two principal sources: nonuniformities in dark current from pixel to pixel, and nonuniformities in electrically-introduced fat zero charge from column to column of the imager. Nonuniformities in dark current will be aggravated by using long exposure times. As explained previously, this fact dictates cooling the sensor to reduce dark current to acceptable levels. Nonuniformities in electrically-introduced charge may be obviated by the use of the buried channel structure proposed for the sensors to be fabricated during the Development Program. However, initial experimental work at TI with buried channel devices suggests that a small background charge, or "slim zero", may still be required. When the sensor is cooled to -40°C, this background charge would have to be introduced electrically, opening the possibility of nonuniformities in this charge level from column to column. The floating diffusion inputs at the top of each column of the proposed imager design provide a means for introducing this background charge in a fairly uniform fashion.

5.   Clocking Waveform

The clocking waveform that will be used is the simple 3-phase sequence described in Appendix A. The choice of a 3-phase structure, as explained above, was based principally on device geometry and area considerations. From an operational point of view, the 3-phase waveform is fairly simple to implement with a few logic gates, and has been used on a number of TI area imagers.

H.   Exposure Procedure

The use of mechanical shuttering has been recommended for this application. This decision is in keeping with the general guideline that has been adopted of providing a sensor that is smaller, lighter, and that consumes less power than a conventional silicon vidicon, but that does not necessarily have any additional frills, such as blooming control or electronic shuttering. The present state of CCD technology is such that a 0.5" x 0.5" chip is about the limiting size that can be fabricated with reasonable yield. Furthermore, the lower limit on pixel size is a little less than 1 mil. When allowances are made for clearance between bond pads and the thinned area of the imager, the maximum area available for the CCD will accommodate an array measuring about 400 x 400 pixels. This size just approaches that of commercial TV. Were the array cut in half to provide an on-chip storage buffer for electronic shuttering, there would be only 200 x 400 pixels in the optically active area. Because of the requirement for slow data readout, it is not possible to interlace the picture to recover the lost 200 x 400 pixels. The slow data readout would require waiting too long between consecutive exposures for the two interlaced fields to "see" the same scene if the spacecraft motion is not stabilized relative to the scene.

I. Expansion To Low-Light Level

The design that has been adopted is ideally suited to low-light-level imaging. As discussed in Sections III.H. and III.I., the signal-to-noise ratio for the proposed sensor at an exposure of 100 $\mu J/m^2$ should be at least 18:1, and will probably be considerably higher. Very little else could be done to the CCD to improve its sensitivity at low light levels. However, a significant improvement in the sensitivity of the camera system could be realized by utilizing the CCD as the target in an electron bombarded silicon (EBS) tube configuration. Such a sensor system is predicted to be essentially photon-noise limited in its sensitivity, and represents the ultimate in very low-light-level performance. The thinned, backside-illuminated CCD structure is easily incorporated in an EBS configuration, as there need be no layers of insulator or resistive sea material on the bombarded surface, that would interfere with electrons incident from the photocathode. Thus, the EBS-CCD represents a logical extension of the proposed sensor design to very low-light-level operation.

SECTION V

PERTINENT EXPERIMENTAL RESULTS

A. Thinning

Recent developmental work at TI under other programs on the proprietary CCD thinning process has yielded significant achievements in this area. It has been possible to thin long (500 elements) linear shift registers over a length of about 400 pixels to a thickness of about 12 μm. The thinned arrays have been operated as imagers, and have performed quite well. The thinning operation has been shown to have no significant effect on either the CTE or the dark current of the thinned devices. Thus, double-level metallization with thinning and backside-illumination has been demonstrated to be a viable technique for CCD imaging.

B. Charge Transfer Effeciency

1. Versus Cooling

In a set of experimental measurements made during the course of this contract, the effect on CTE of cooling a surface-channel CCD sensor and lowering its clock frequency was studied. Lowering the temperature from 300 K to about 100 K had very little effect on CTE. Some slight improvement in CTE was seen, but it was within the range of experimental error.

2. Versus Frequency

The results of lowering the output pixel rate from 100 KHz to 100 Hz are shown in Figure 5-1. The slight increase plotted in CTE at low frequencies is within the range of possible experimental error. Thus, no decrease in CTE at low frequencies down to 100 Hz was observed, in contrast with the theoretical predictions of Melen and Meindl* for surface-channel CCD's. Sufficient electrical fat zero was introduced at each frequency to symmetrize the output pulse train waveform, the distinguishing attribute of a true proportional loss, which is the only type of loss that can be characterized by a constant CTE (percent loss independent of signal level). The amount of fat zero required was not measured, so it is not known how much fixed loss was present.

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*R.D. Melen and J.D. Meindl, "A Transparent-Electrode CCD Image Sensor," presented at the 1973 IEEE Solid State Circuits Conference, Philadelphia, February 15, 1973.

10^{-2}

ϵ

10^{-3}

10^2 10^3 10^4 10^5

f_c (HZ)
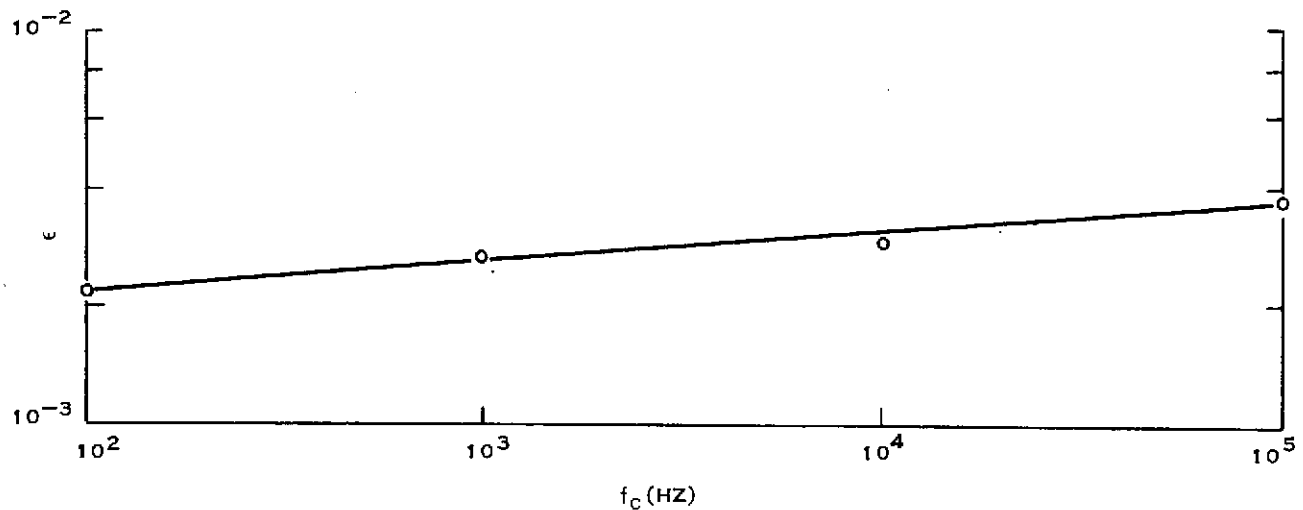
**Figure 5-1. Transfer Inefficiency (ϵ) Versus Frequency (f_c) for the
Output Serial Register of a 64 x 64 CCD Array**

C.   Fixed Pattern Interference

Photographs were taken using a 64 x 64 CCD imager at a temperature of 300 K, and again at about 100 K. The results are shown in Figure 5-2. The sensor had such a high incidence of leakage current spikes that practically no image is discernible through the fixed pattern interference at 300 K. When cooled, however, the sensor display looked quite good, as shown in Figure 5-2b.

Measurements were also made of the uniformity from channel to channel of the electrically-introduced fat zero level in a 64 x 64 array with floating diffusion inputs at the top of each parallel channel. One output video line is shown in Figure 5-3. The average fat zero level for this measurement was about 27% of a full well. The rms nonuniformity in fat zero level is estimated from the figure to be about 10%, expressed as a percentage of the mean fat zero level. For this measurement, the Fat Zero Load Gate (See Figure 2-1.) was pulsed on and off to charge the floating diffusions to the potential applied to the Fat Zero Reference Diode. This technique has the disadvantage that variations from channel to channel in threshold voltage near the floating diffusions will result in variations of the quantity of fat zero charge introduced. This deficiency may be remedied by applying the reference voltage to the Fat Zero Load Gate and pulsing the Fat Zero Reference Diode to a low voltage and back to a high voltage (Reference 67). This technique should be investigated in further experiments.
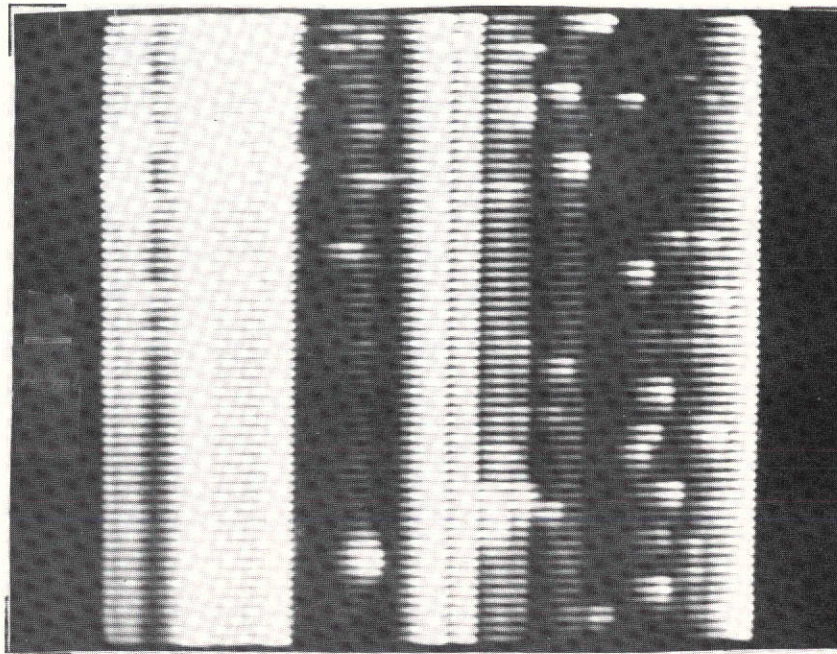
(A) UNCOOLED
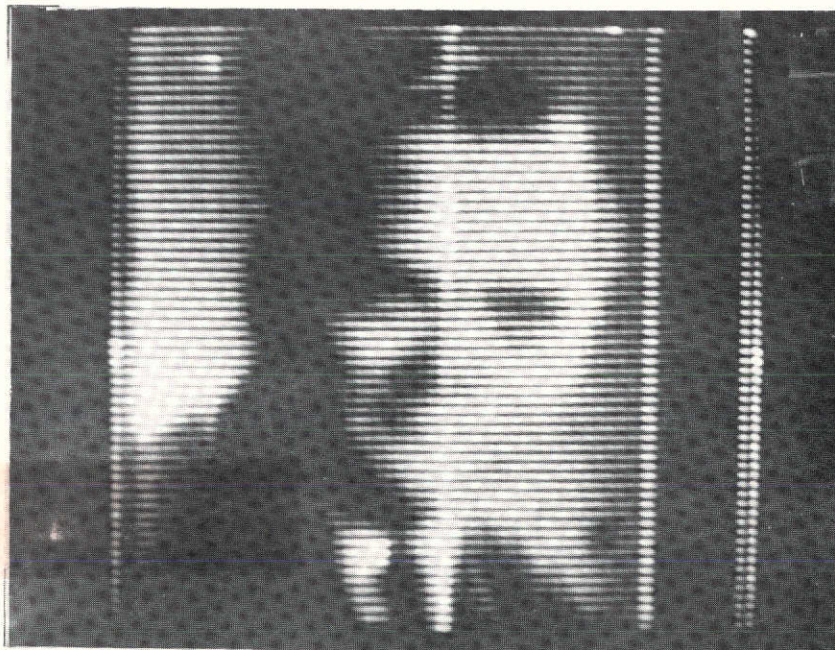
(B) COOLED

Figure 5-2. Fixed Pattern Interference in a 64 x 64 CCD

FULL WELL LEVEL →

ZERO CHARGE LEVEL →
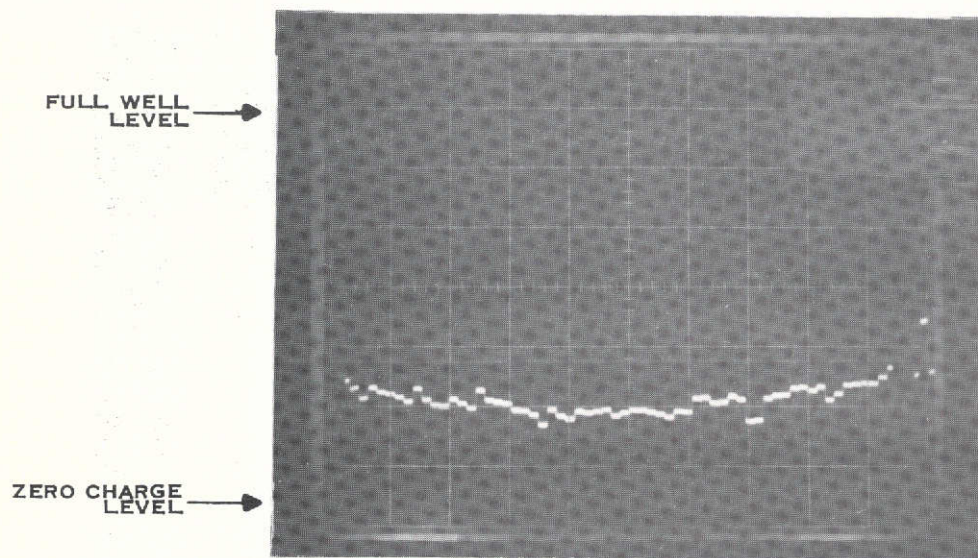
Figure 5-3. Fat Zero Nonuniformity in a 64 x 64 CCD with
Parallel Floating Diffusion Inputs

APPENDIX A

FUNDAMENTALS OF CHARGE-COUPLED IMAGERS

I. Introduction

A charge-coupled device, when used as an image sensor, operates by the transfer in unison of several disjoined quantities of electrical charge along a line of closely-spaced MOS capacitors. The transfer, which in one sense is a propagation of charges, is accomplished by the application of appropriate voltage pulses, which are called clocking signals, to the electrodes forming the capacitors. This is the bucket-brigate concept that has been known for many years as a type of electronic circuit; but the subject aroused little excitement. However, after Sangster and Teer (48) and Boyle and Smith (11), independently, pointed out relatively simple, integrated-circuit implementations of the principle a great interest has been shown. The simplicity, potentially high density, low power requirements, and inherently low noise of these all solid-state devices make them attractive for a number of applications among which are self-scanned photosensor arrays having potentially large dynamic range. Small size, shock resistance, fast turnon, and insensitivity to strong electromagnetic fields are other beneficial aspects.

The capacitors are of the metal-oxide-semiconductor, MOS (metal insulator semiconductor, MIS) structures common to many integrated circuit devices. One row of capacitors is the CCD linear array. In principle, a number of linear arrays assembled and operated in parallel constitute the CCD area array.

II. Simple CCI Concept

The charge — minority carriers which are either electrons or holes — accumulates, that is, is stored in spatially defined depletion regions, or potential wells, created at the surface of the semiconductor by voltages applied to the capacitor electrodes. The device is illustrated in Figure A-1 by the cut-away view of a 3-phase, single level metal, surface channel device. The figure shows the stored negative charge (electrons) under the middle electrode, which is biased to a more positive voltage than the two adjacent electrodes. The structure is simple, consisting of a lightly doped p-type silicon substrate with a silicon dioxide layer formed on its surface and finally with the pattern of metal electrodes formed on the SiO_2 surface. The three full-size electrodes shown constitute one unit cell, or pixel, of the 3-phase array.

The quantity of charge in one potential well is referred to as a charge packet; however, it is actually more like a flock. When a "flock" is transferred from one well to the next, stragglers and charges that get lost on the way in interface energy states have to be contended with. For example, let us assume that we start with 10,000 electrons in a well and that this particular flock must be transferred 2000 times before it leaves the array to become one of a series of pulses forming the video signal. If on the average only one electron is lost per transfer, then only 8,000 of the original 10,000 are left. The flock that we are watching will of course pick up some charges lost from flocks that precede it to the output. However, this intermingling of the flocks causes problems that are discussed in other parts of this report under the topics of "charge transfer inefficiency" and "surface state trapping."
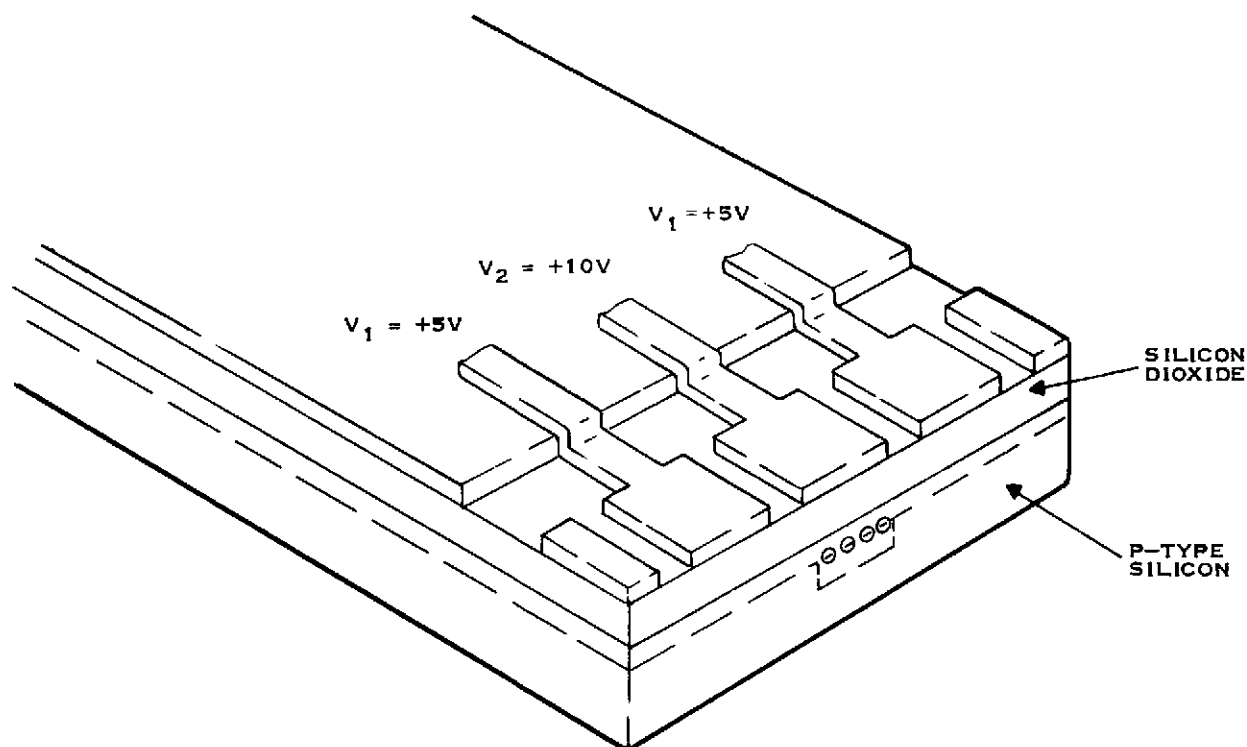
Figure A-1. Cut-Away of a 3-Phase, Single Level Metal, Surface Channel Charge-Coupled Device

For the most part, in this appendix, only the simple, single level, 3-phase, surface channel device is discussed; most of the structural variations that have been reported are discussed in other parts of this report. Use of the word "packet" will be resumed because it is conventional; and its connotation of being wrapped up together and tied does give a better feeling.

In a CCD image sensor (CCI), electron-hole pairs are created in the bulk material by the absorption of incident photons; the minority carriers migrate by diffusion and the influence of electric fields to the potential wells. The size of a packet is therefore proportional to the quantity of light flux incident on the semiconductor surface near that well.

III. Energy Level Diagram

In order to understand better how the wells are formed let us now study the potential energy diagram for the MOS structure which is shown in Figure A-2. The Fermi energy of the metal appears on the left; on the right the band edges of the insulator and semiconductor are shown as functions of distance perpendicular to the surface. On the far right the Fermi level in the p-type semiconductor is shown. The bias voltage V_G is the applied potential difference between the semiconductor and metal. Figure A-2a shows the potential distribution in the absence of collected minority carriers; Figure A-2b illustrates the potential distribution after a sufficient number of minority carriers have collected at the interface. The latter is the steady-state condition for the structure. Any further introduction of electrons will cause the interface potential to become yet more negative and electrons will be injected into the bulk — where they will recombine — until the
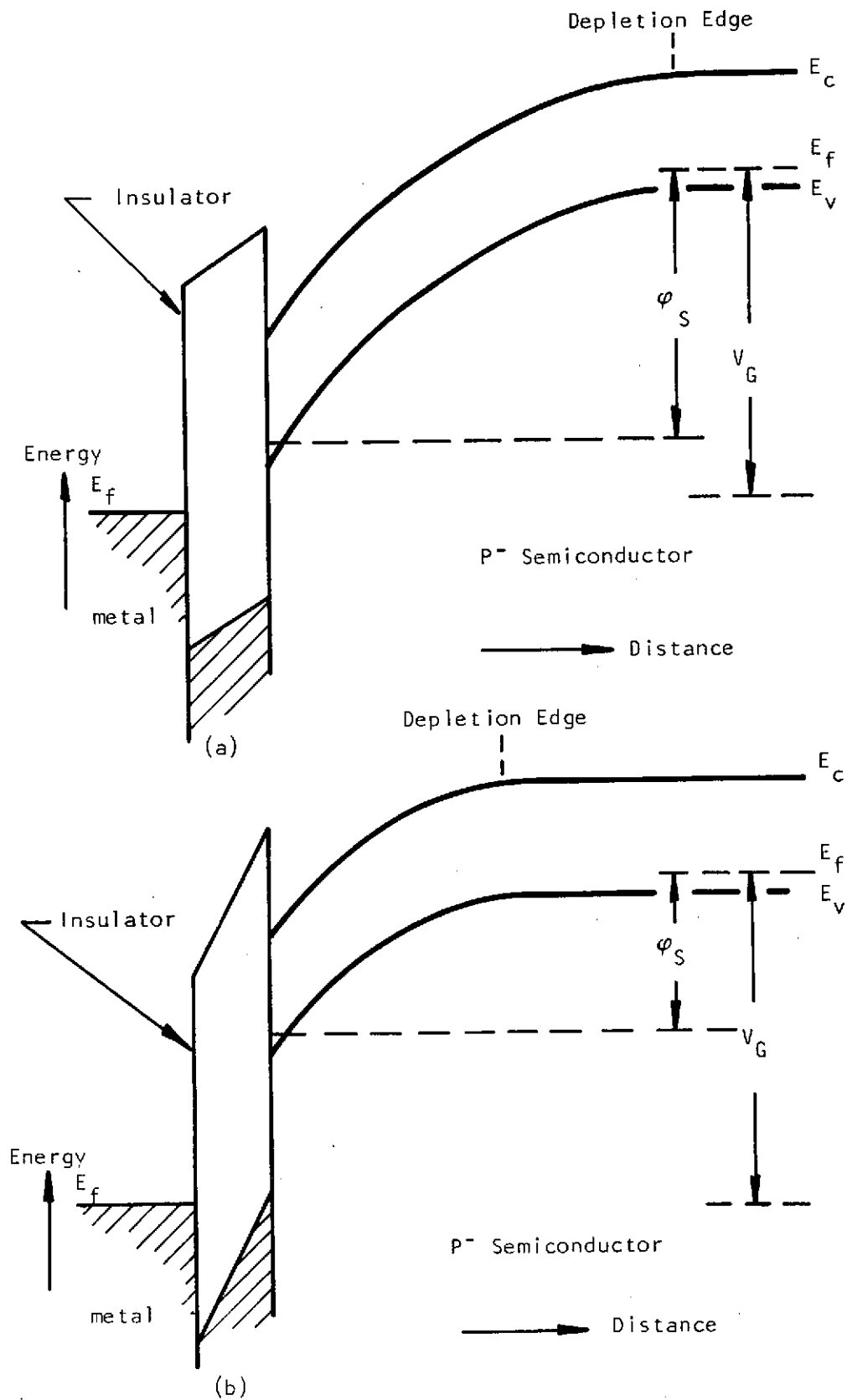
Figure A-2. Energy Level Diagram of a Metal Oxide P-Type Semiconductor Combination

steady-state condition is again reached. With the collection of minority carriers in the depletion well, the depletion width decreases as shown in the diagram; therefore, as will be explained in greater detail later, the differential capacitance increases and, as shown, the magnitude of the surface potential φ_s decreases. The quantity of minority carriers held at the interface cannot change with rapid changes in electrode to bulk voltage. The capacitance characteristics are dependent on the removal or addition of mobile charges at the depletion edge as the electrode bias is increased or decreased.

Figure A-1 shows a p-type bulk (minority carriers are electrons) device in a situation where a sufficiently large positive bias potential has been applied to all the electrodes to produce inversion, and the center electrode has a slightly larger applied potential. There is no inversion layer, which would imply the presence of charges at the surface, only depletion, because a negligible number of minority carriers are present. This is not a steady-state situation; nevertheless, because present silicon art produces material with low densities of surface and bulk generation centers, the surface will remain depleted for times of the order of seconds before enough thermally generated minority carriers accumulate to reach the steady-state. If minority carriers are introduced through any one of several means, as by the absorption of photons, they will collect at the surface in the potential maximum defined by the excess potential on the central electrode.

IV. Three-Phase Transfer Scheme

A study of the 3-phase clocking scheme, which will now be undertaken, will disclose how the transfer of charge takes place. The three phases, used in the example being considered, allow a preferred direction to be established so that a charge packet will move in the desired transfer direction each time it leaves a well. In the 3-phase structure, when charge is transferred from one electrode to the next, the electrode behind the one transferring charge is kept at a potential that repels the free charge and thereby prevents backward flow. The electrode to receive charge, meanwhile, is made more attractive to charge than the one giving up its charge. It can be seen that this arrangement requires three electrodes (at least) for each packet of charge and that each electrode must be driven by a separate clock line.

Let us consider the linear array of MOS structures illustrated schematically in Figure A-3. Every third electrode is connected to a common conductor. In the initial condition, a voltage $+V_2$ is applied to electrodes 1, 4, 7, and so on, and a voltage $+V_1$ with ($V_2 > V_1$) is applied to the other electrodes. The semiconductor is held at zero voltage. It is assumed that $V_1 > V_T$ where V_T is the threshold voltage for the production of inversion under the steady-state condition. The edge of the depletion region is indicated by the dashed line. Also, as an example, negative charge is shown under electrodes 1 and 7 and none under electrode 4, as indicated in Figure A-3a. If a voltage V_3 with ($V_3 > V_2$) is applied to electrodes 2, 5, 8, and so on, as shown in Figure A-3b, the charge will transfer from electrodes 1 and 7 to electrodes 2 and 8 respectively. The charges will have been shifted one position; and the voltages would then normally be returned to the condition shown in Figure A-3c with the voltage V_2 applied to electrodes 2, 5, 8, and so on, and the voltage V_1 to the others. The charges can be transferred one step further by the application of a similar sequence of clocking voltages beginning with the application of V_3 to electrodes 3, 6, 9, and so on. Three sequences of clock pulses move a packet a distance equal to one pixel. In actual practice, only two voltage levels are usually used. Then Figure A-3b would represent the instantaneous condition of the depletion regions after electrodes 2, 5, and 8 have been switched to the more positive of the two levels, and while the potential on electrodes 1, 4, and 7 is falling back to the less positive level.
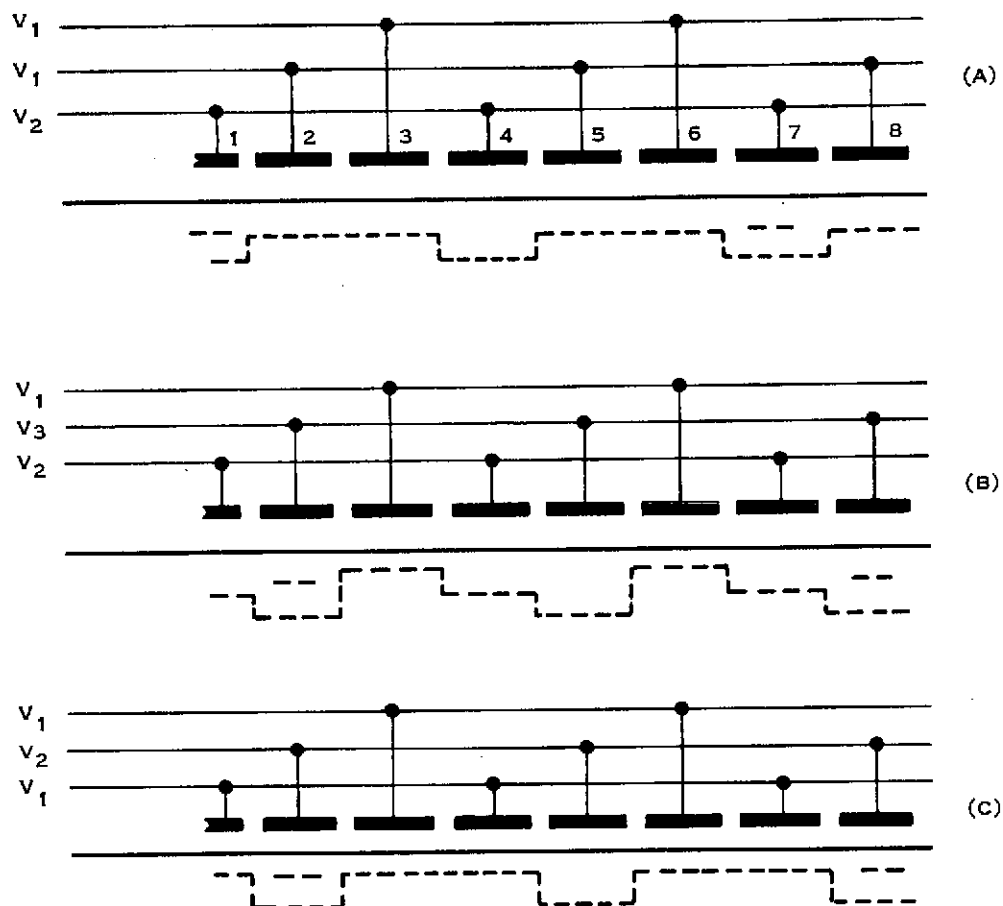
Figure A-3. A Three-Phase Transfer Scheme for a Charge-Coupled Device

In an image sensor, the quantity of charge that accumulates in any given well must depend on the rate of electron-hole generation by photon absorption in the bulk material and on the integration time, t_g, during which the minority carriers are allowed to accumulate. One way to regulate the integration time is by using an optical shutter. Pair generation by other processes, for example, by absorption of thermal photons, must be slow when compared with photon generation. Generation by other processes must also be slow when considering the integration time and the time required to read all the charges out of the array. Let us illustrate with the example discussed in the following paragraph.

A full frame, 3-phase device of 500 x 500 pixels is to be read out at the rate of 10^6 master clock pulses per second (3.3×10^5 pixels per second). The device is so designed that 3 clock pulses shift all 500 vertical channels in unison downward a distance equal to one pixel size. The bottom

horizontal row of charges are shifted out to a horizontal serial register. This first row of charges is shifted out of the serial register horizontally by a different 3-phase clocking system to a readout circuit consisting of a precharge amplifier, which is described elsewhere. After the packets in the serial register are read out, the packets remaining in the array are shifted downward one more step. Four clock pulses are required to remove the first charge packet; but the last packet in the array to be read out requires 7.5×10^5 clock cycles. At the master clocking rate of 10^6 Hz this last packet is in some well or in transition between wells for 0.75 second minus the short time to read the last row out of the serial register. The readout time t_r, in this case 0.75 second, is the time required to read one complete set of charges out of the array. If the packets accumulate a significant quantity of thermally generated charge during readout, this extra charge will cause the upper part of the reconstructed image to be brighter and more noisy than the lower part.

V. Voltage-Capacitance Relations

Charge-coupled devices are frequency limited at both the high and low end of the useful range of frequencies, at the high end by charge transfer inefficiency and at the low end by thermal generation of minority carriers. To understand the low frequency limitation one needs to understand the relationships between capacitance and voltage in the ideal MOS structure and the effects of frequency. Hence, a brief explanation of the MOS capacitance is given in the following paragraphs. Charge transfer inefficiency is discussed in another section.

Each electrode together with the ohmic contact at the base of the substrate, forms a capacitor. The effective capacitance C of one capacitor is actually the capacitance of the series combination of two capacitors: the capacitance C_O of the insulator (oxide layer) and the capacitance C_D of the space charge (depletion) region of the silicon (Ref. 27, p. 271 and Ref. 56, p. 433):

$$C = C_o C_D / (C_o + C_D).$$ (1)

The oxide capacitance per unit area is normally much larger than the depletion capacitance and is given by

$$C_o = K_o \epsilon_o / d,$$ (2)

where K_o is the dielectric constant for the oxide layer, ϵ_o is the permitivity of free space, and d is the oxide thickness. For a 1200 Å thick SiO_2 layer, C_o would be approximately 2.8×10^{-8} F cm^{-2}. The stored charge is divided between the two capacitors to given an instantaneous surface potential φ_s.

The capacitance of an ideal MOS system as a function of the gate voltage V_G applied to the electrode is described graphically by the curves of Figure A-4. Let us study the curves beginning at the left (with a gate voltage negative with respect to the p-type substrate) so that in the steady-state there would be an accumulation of holes at the interface. The effective capacitance is high, being close to that of the oxide layer C. At $V_G = 0$, the capacitance would be that for the flat band condition (we shall assume a zero flat-band voltage). See Figure A-5. If the negative voltage is reduced (made sufficiently more positive), a depletion region, which acts as a dielectric layer in series with the insulator, is formed near the semiconductor surface; and the total capacitance decreases because of the series combination of two capacitors. The effective capacitance goes through a minimum and then increases again as the inversion layer of electrons forms at the
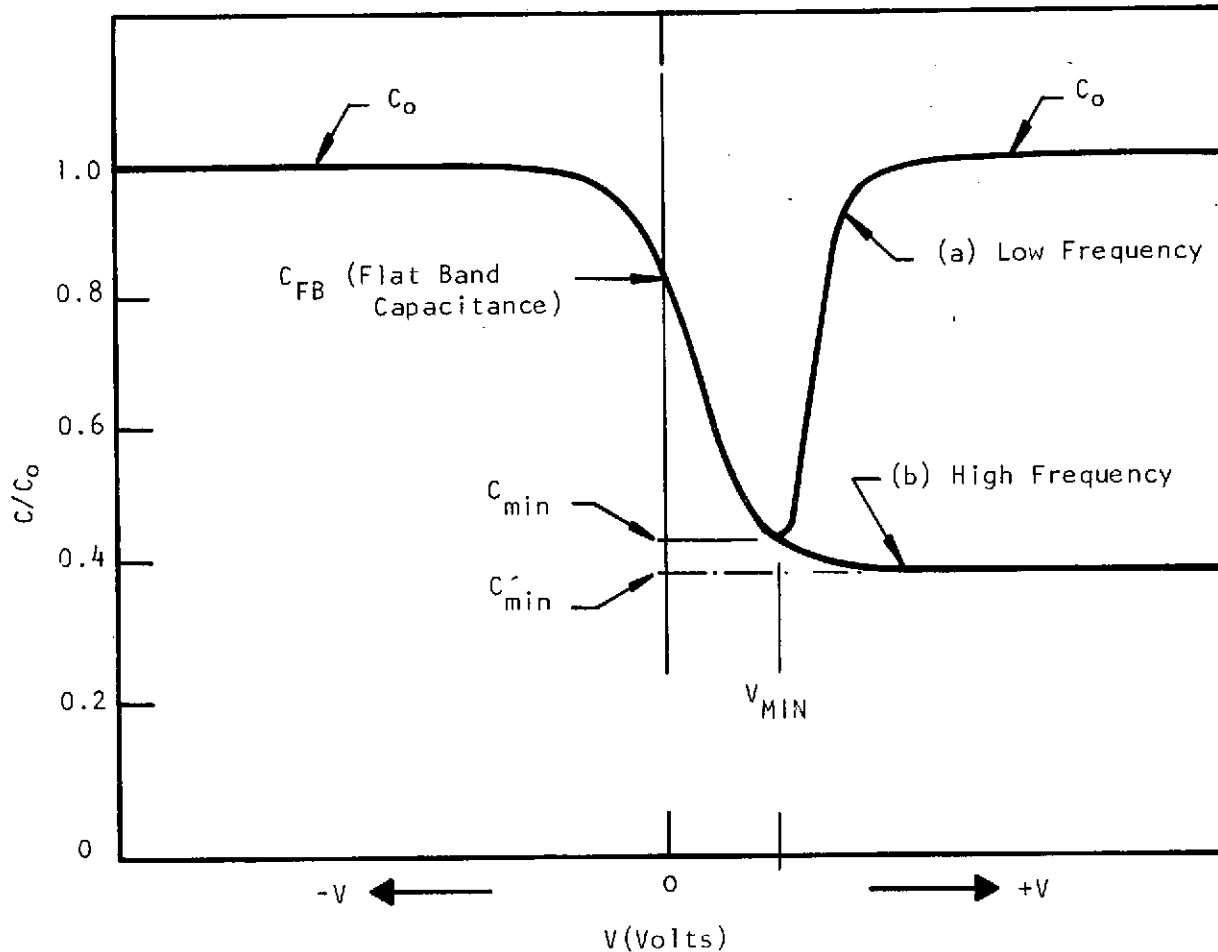
Figure A-4. MOS Capacitance-Voltage Curves

interface, that is, the potential wells become partially filled, and the depletion region decreases and the capacitance increases.

During the operation of a CCI when V_G is changing with the clocking signals, the increase of capacitance is dependent on the ability of the electron concentration to follow the changes of the applied voltage. This is only possible at low frequencies such that the recombination-generation rates of the minority carriers can keep up with small
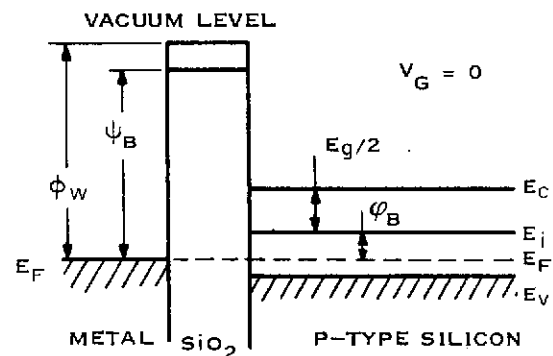
Figure A-5. Energy-Level Diagram for an Ideal MOS Structure When the Electrode Voltage V_G is Equal to Zero for a P-Type Silicon Substrate

signal variation and allow for charge exchange with the inversion layer in step with clocking signals. Experimentally, for thermal generation-recombination at room temperature, it has been found that the low frequency condition is from a fraction of a hertz to a few tens of hertz. As a consequence, MOS curves measured at high frequencies do not show the increase of capacitance, as shown on the right of Figure A-4. Figure A-6 shows the change of the capacitance-voltage curves for four different frequencies, illustrating the high and low frequency cases for a device near room temperature. An increase of temperature of the device causes it to reach the "low frequency condition" at a higher frequency.

In the case of a CCI, it is possible for two different rates to apply. During exposure to light while inversion charges are accumulating at the interface, it is the optical rate for photon absorption that applies. After a mechanical optical shutter is closed, and before the charges are read out of the array so that the device is "at rest" in the dark, it is the thermal rate that applies.

When the semiconductor surface is depleted, the quantity of charge per unit area in the depletion region is given by ($-qN_AW$) where W is the depletion width. Integration of Poisson's equation yields the potential distribution with distance x into the semiconductor (Ref. 27, p. 267 and Ref. 56, p. 436):

$$\varphi = \varphi_s \left[1 - (x/W) \right]^2 , \tag{3}$$

where the surface potential φ_s, which represents the amount of bending of the bands as shown in Figures A-2 and A-5 from the bulk of the semiconductor to the interface, is given by

$$\varphi_s = qN_AW^2 / 2K_s\epsilon_0 . \tag{4}$$

In these expressions, N_A is the accepter ion concentration, K_s is the dielectric constant of the semiconductor, and q is the electronic charge. When the applied voltage increases, φ_s increases, and so does W. Eventually strong inversion begins when φ_s (inv) = $2\varphi_B$ occurs. φ_B is the potential
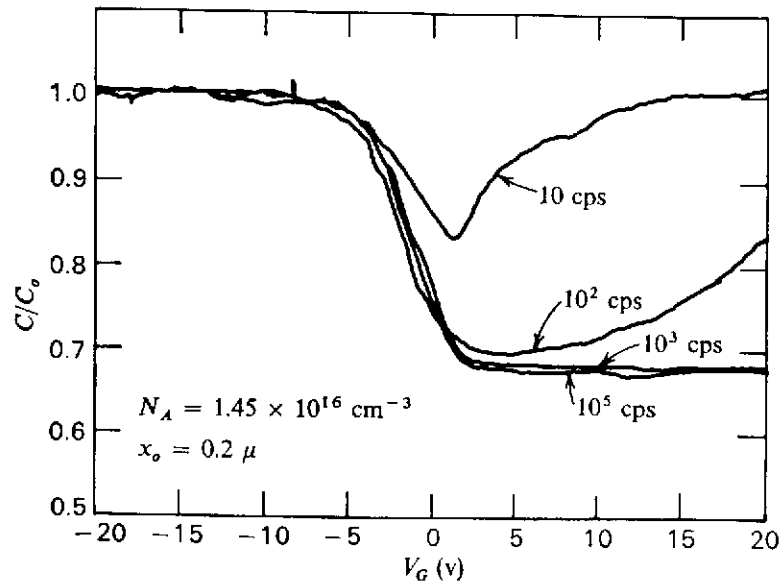
Figure A-6. The Capacitance-Voltage Characteristic for an MOS Structure
Showing the Effects of Measurement Frequency (Reference 28)

difference between the Fermi level E_f and the intrinsic Fermi level E_i. Once strong inversion occurs, the depletion layer width reaches a maximum. When the bands are bent down far enough that $\varphi_s = 2\varphi_B$ the semiconductor is effectively shielded by further penetration of electric field by the inversion layer and even a very small increase in band bending will result in a very large increase in the charge density within the inversion layer. Accordingly, the maximum width W_m, of the surface depletion region can be obtained from the equations above.

$$W_m = \sqrt{\frac{2K_s\epsilon_o\varphi_s(\text{inv})}{q\,N_A}} \tag{5}$$

VI. Charge-Potential Relations

The surface potential φ_s, which appeared often in the preceding section, is not only related to the capacitance but is also related to the applied electrode potentials and to the charge that accumulates. A study of these relationships can help us understand and determine the magnitudes of voltages necessary to create the potential wells and clock out the charges.

The relationship between potential and charge is obtained by solving Poisson's equation (Ref. 2):

$$\Delta^2 V = \frac{-\rho}{\epsilon} = \frac{q}{\epsilon}(N_A - N_D + n - p), \tag{6}$$

where N_D and N_A are the donor and acceptor concentrations and n and p are the electron and hole densities. Typically, in approaching an MOS problem the three-dimensional Laplacian is replaced by a one-dimensional second derivative. The justification for such a simplifying reduction is that the capacitor is "large" and the variations in potential along the surface may be ignored. This procedure is followed to present the basic ideas of charge and potential in a CCI; however, for regions near the perimeter of the capacitor the one-dimensional formalism is likely to be quantitatively in error. In addition, the depletion approximation is employed which calls for strict application of the Poisson equation in the depleted region and the Laplace equation in the neutral bulk. Electron and hole densities are ignored except for any surface charge present at the interface.

Upon the instantaneous application of a voltage V_G to the electrode, a depletion region is formed in the semi-conductor. The gate voltage V_G is then related to the potential at the surface φ_s by

$$V_G - V_{FB} = \varphi_s + \frac{1}{C_o}(2K_s\,\epsilon_o\,q\,N\,\varphi_s)^{1/2} \tag{7}$$

where V_{FB} is the flat band voltage and N is the doping density. The flat band voltage V_{FB} is given by

$$V_{FB} = \phi_{MS} - \frac{1}{C_o d}\int_0^d x\rho(x)\,dx = \phi_{MS} - \frac{Q_{ss}}{C_o}, \tag{8}$$

where Q_{SS} is an effective surface charge density to account for the volume charge density $\rho(x)$ distributed throughout the insulator of thickness d, and ϕ_{MS} is the metal-semiconductor contact potential difference. Now, if in addition to this effective oxide charge, we add a charge density q_o at the interface resulting from the formation of an inversion layer, the potential is altered by a term q_o/C_o. Including this term and solving for the surface potential gives

$$\varphi_s = V_o + V - (V_o{}^2 + 2VV_o)^{1/2} , \qquad (9)$$

where

$$V = V_G - V_{FB} - \frac{q_o}{C_o}, \qquad (10)$$

$$V_o = \frac{K_o \epsilon_o \, qN}{C_o{}^2} . \qquad (11)$$

The surface potential φ_s is of overriding importance in a discussion of CCD operation and will be referred to frequently. For convenience, φ_s is plotted as a function of V in Figure A-7 with N and d as parameters. Note that for large V (corresponding to a large depletion depth and small depletion capacitance) the curves become linear with a slope of one.

VII. Surface States

The incomplete transfer of charge is a phenomenon of great moment in CCI's because it ultimately limits both the maximum number of allowed transfers and the high frequency limit for the clocking pulses. There are several contributions to the incomplete transfer, but one that is most prominent and the only one discussed in this Appendix is the loss caused by trapping of minority carriers by surface, or interface states. Since a discussion of surface states consequently precedes a discussion of transfer inefficiency, the discussion of surface states follows immediately.

In a practical MOS device, in addition to the normal energy states shown in Figures A-2 and A-5 and in addition to the charges that appear in the accumulation, depletion, and inversion regions, there exist many other states and charges which will, in one way or another, affect the ideal MOS characteristic. The basic classification of these states and charges are shown in Figure A-8. There are (1) surface states or interface states which are
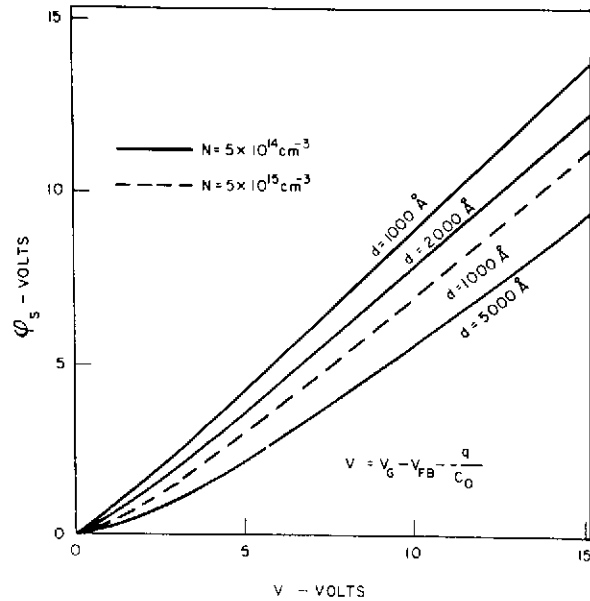
Figure A-7. Potential at the Interface of a CCD as a Function of Applied Electrode Voltage (Reference 2)

METAL

S_iO_2

⊞ FIXED SURFACE CHARGES

✕ SURFACE STATES

⊕ IONIZED TRAPS

N_a^+ MOBILE IONS
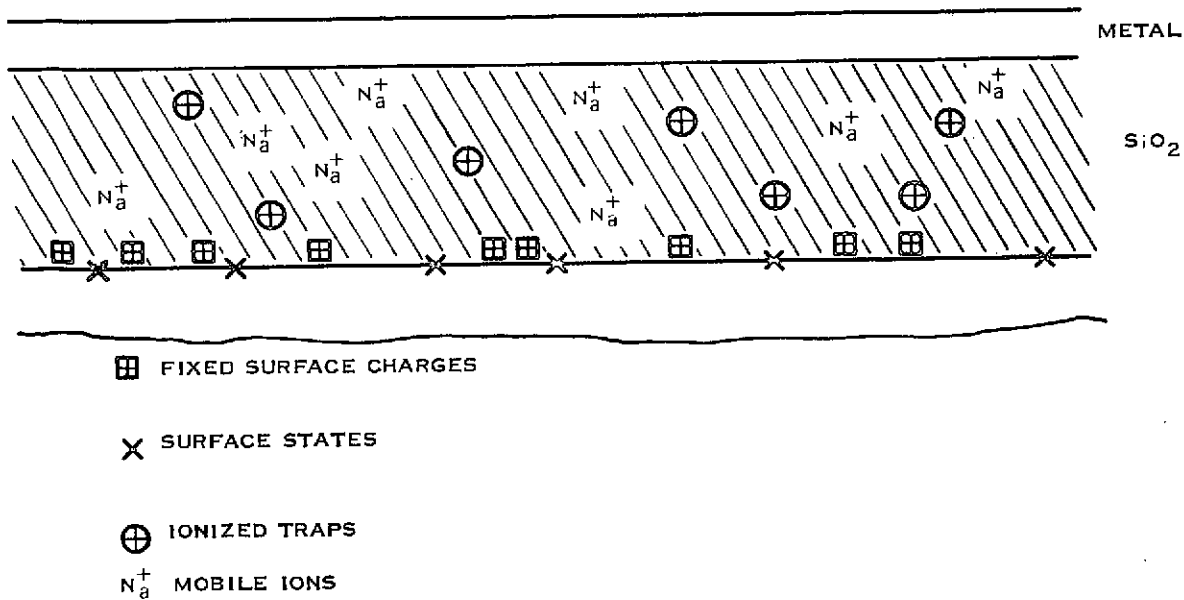
Figure A-8. Energy States and Electric Charges in the Oxide Layer of a CCD

defined as energy levels within the forbidden band gap at the insulator-semiconductor interface which can exchange charges with the semiconductor in a short time, (2) fixed surface charges which are located near or at the semiconductor surface (~ 200 Å) and are immobile under applied electric fields, (3) mobile ions such as sodium which are mobile within the insulator under bias-temperature aging conditions, and (4) ionized traps which can be created, for example, by x-ray radiation.

The surface states have been studied extensively and have been shown to exist within the forbidden gap due to the interruption of the periodic lattice structures at the surface of a crystal. Measurements on clean surfaces in an ultrahigh vacuum system have confirmed that the density of surface states is very high — of the order of the density of surface atoms. Historically, surface states have been classified into fast and slow states. The fast states exchange charge with the conduction or valence band rapidly, and are assumed to lie close to the interface between the semiconductor and the insulator. Slow states, on the other hand, exist at the interface of the air and insulator and require a longer time for charge exchange. For MOS devices with thick insulating layers, the only states that we are concerned with are the interface states at the insulator-semiconductor interface. And these states are not necessarily fast surface states either, since at low temperatures, the time constant of these states is relatively very long. A surface state is considered as a donor state if it can be neutral or it can become positive by donating (giving up) an electron. For an acceptor surface state, it can be neutral or it can become negative by accepting an electron. When a voltage is applied, the surface levels will move up or down with the valence and conductance bands while the Fermi level remains fixed. The probability of the occupation of surface states will change when the amount of band bending is changed. Thus, the charge in the fast surface states will vary with the

band bending or surface potential φ_S. A change of charge will also contribute to the MOS capacitance and will alter the ideal MOS curve.

VIII. Transfer Efficiency

A fundamental requirement for a self-scanned imaging device is that it exhibits an analog, and preferably linear, behavior, that is, that the size of a charge packet — when measured at the output and attributed to a specific light-sensitive element — be directly related to the integrated light intensity incident on that element. Except for the charge that may be left behind or lost during charge transfer, CCI's inherently have this linear analog behavior. The transfer efficiency is the percentage of charge remaining in the original packet after transfer along the device. See References 2, 10, 21, 42, and 55. Transfer inefficiency as a percent is 100 minus the efficiency. Because of the loss of charge, the video signal will be attenuated; the spatial resolution (or MTF which is discussed in another part of this report) will be degraded; and the total number of transfers for useful operation will be limited. Hence, the mechanisms that inhibit the transfer of charge are of special interest.

Transfer efficiency is related to at least two factors: One is the dynamics of the minority carriers as they move by diffusion and drift from one well to the next. The second involves trapping of charges in fast interface states. The rate at which the charges move is governed by both diffusion processes and the tangential electric field at the surface. The tangential field is determined by the electrode voltages and the electrode structure and spacing and will dominate the transfer rate in a well-designed configuration. Use of minority carriers with the highest mobility, electrons in the case of silicon, speeds the charge motion. One advantage of buried channel (which is not discussed in this appendix) is that the carrier mobility is higher in the bulk of the buried channel than along the surface of the simple, surface channel device.

It has been observed experimentally that part of the charge packet appears to transfer rapidly, whereas some lesser charge density, say a fraction f of the maximum charge density, transfers more slowly with an exponential time constant τ. Since, at the frequencies on the order of a few megahertz required in imaging devices, the time available for transfer is much greater than the duration of the rapid transfer behavior, the efficiency η is essentially governed by the fraction f and the slow time constant τ. Thus, after time t

$$\eta \approx 1 - fe^{-t/\tau}. \tag{12}$$

This kind of behavior has been confirmed not only by experiment but also by analytical studies and by computer modeling. Ignoring for a moment the effects of tangential surface fields, the behavior is qualitatively easy to understand. At time t = 0, the beginning of the transfer, the packet is very dense and localized, and the gradient of the carrier density at the edges of the packet is large. When the surface potential of the adjacent electrode becomes more positive than the local potential, namely, when the adjacent MOS structures couple, a considerable fraction of the packet transfers very quickly due to the strong repulsive forces felt by these electrons. As time evolves, this repulsive force decreases and becomes asymptotic to a value given by considerations of thermal diffusion and surface electric field intensity. This determines the time constant τ in the equation above, and f is an empirically defined quantity reflecting the density below which the electrons do not "feel" the presence of the other electrons. A detailed presentation of this behavior has been given in Reference 55. The results indicate, for example, that a transfer efficiency of 99.99 percent per transfer can be expected from a device with 10 μm electrodes operated at 1 MHz.

One important impediment to charge transfer is inadequate coupling across the region below the interelectrode gap. This condition results from too large an electrode separation for the operating voltage used and/or from a detrimental concentration of oxide charge in the gap region possessing the same sign as the minority carriers. One obvious way of circumventing these difficulties is to eliminate the gap altogether by using overlapping electrodes. The interelectrode gaps and the oxide charge of the same polarity as the stored charge should be kept "small." Since silicon dioxide tends to charge positively, use of a p-type silicon substrate is most advantageous. In this case the surface tends to be positive with respect to the neutral bulk and aids in the depletion of the surface. Similarly, when the gaps are large there is more charge in this region to be swept out in order to achieve depletion and, consequently, less coupling. Empirically, it has been observed that for interelectrode gaps on the order of 3 μm and oxide charge densities on the order of 10^{11} cm^{-2}, satisfactory coupling can be achieved using peak voltages of less than 10V.

Another mechanism whereby transfer efficiency may be reduced is the temporary trapping and re-emission of the minority carriers at a later time by surface states. The carriers may be trapped in either the lower or the upper half of the bandgap for p- and n-channel devices, respectively. The probability of a state being occupied by a minority carrier depends on the energy level of the state, its relative density, and the density of carriers. When a charge packet moves to the next element, the minority carrier density falls several orders of magnitude and any trapped carriers are then reemitted with a characteristics time depending on the energy difference to the nearest band. If this time is very short compared to the transfer time, the charge is re-emitted into the correct packet and there is no net effect on transfer efficiency, but if it is of the same order of magnitude as the time of transfer or longer, some of the trapped charge is re-emitted into a trailing packet of charge. Since the statistics of trapping is in part a function of the charge density, the addition of a small background charge will reduce the effects of surface states.

The effect of inefficiency in charge transfer is to deteriorate image quality by reducing the modulation transfer function (MTF) or sine wave response and by producing a phase shift for different spatial frequencies. (These are discussed in the main body of this report.) The interpretation of the transfer efficiency in terms of a sine wave input enables the quantitative degradation to be calculated.

IX. Power Requirements

A. Power Dissipation

In well designed CCD's the actual power dissipated is small since there is no dissipation while the device is statically storing charge. Power dissipated by operation on the charges is caused by a finite charge carrier mobility. There will also be resistive losses in the transfer electrodes and power dissipated in the clock pulse drivers.

The total power dissipated on a chip has not been calculated because of the mathematical complexity and a dependence on waveform. However, an estimate of the minimum power has been made from a sinusoidal travelling wave CCD model (Reference 54); the average power dissipation per bit was found to be

$$P_D = QL^2 f_c^2 / \mu. \tag{13}$$

where Q is the signal charge, L is bit length, f_c is clocking frequency, and μ is the mobility. The power P_D from Equation (13) for the case of Q equal to one picacoulomb is plotted in Figure A-9. The dissipation is found to be small indeed, which was expected because currents to the capacitances are principally reactive, not dissipative, currents.

When a CCD is operated at low frequencies, or if for other reasons the device is "passive" for some time with charges stored in the wells, there are two problems that must be considered. First, generation currents originating from interface state or bulk generating centers in the space charge region of the semiconductor will contribute additional charges to the wells and degrade the signal-to-noise ratio. Ultimately, this effect would saturate the wells; consequently, there is a lower limit to the operating frequency. Second, only a small, finite charge is received when a packet is transferred to the output circuits; and any shunt conductance that might render the device inoperative at low frequencies must be avoided.
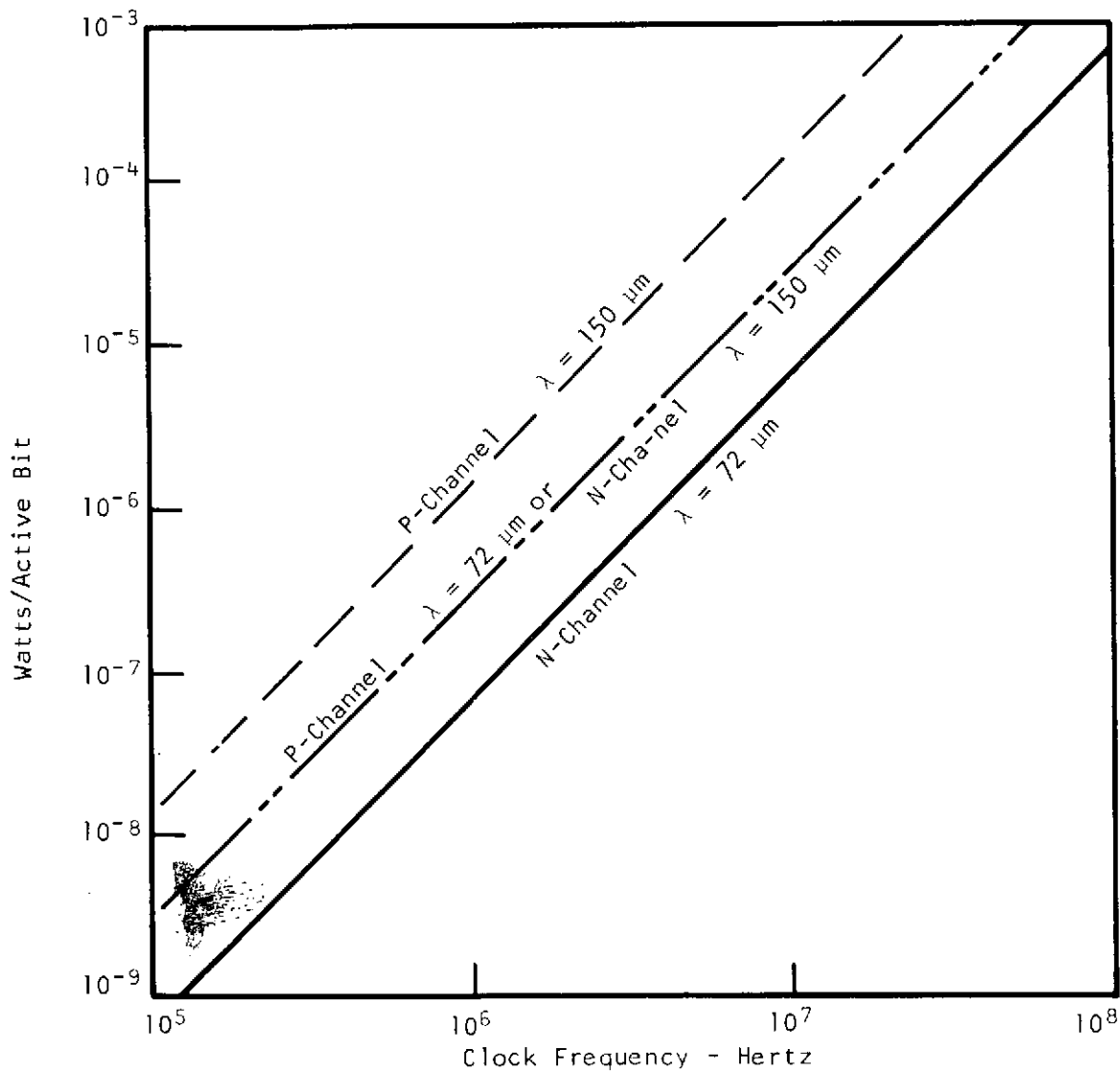

Figure A-9. Real Power per Active Bit for N- and P-Channel CCD's with
Bit Lengths L_p of 72 and 150 μm (Reference 54)

B.   Clock Waveform

Several generalizations can be made about a desirable waveform (see Reference 8, p. 693). Considering the nonlinear charge transfer characteristics, it is found that all contributions to incomplete transfer decrease as the drive voltage is made larger. Hence, it may be concluded that best operation will occur when the largest clock voltage that is compatible with all other requirements is used and when an optimum fraction of that voltage is used for the signal, that is for implementing the transfer of charge. A waveform having a short rise time (for n-channel CCD's) and one that allows a long time interval during which transfer current can flow should be chosen. Figure A-10 shows a computed signal degradation caused by incomplete transfer as a function of frequency for three different waveforms. The advantage of using a waveform with negligible rise time is quite evident.

There is another effect associated with very short fall times in the clock waveform. To illustrate, let us suppose that the time required to change a clock line voltage on an n-channel CCD from its most positive value to its least positive value is negligible compared to the time for most of the charge to transfer from one capacitor to the next. Then if a relatively large quantity of charge were present on a capacitor, the surface potential could be driven negative with respect to the substrate for a short period of time. If this occurred, some of the electrons representing the signal would be injected into the semiconductor bulk where they would be lost to recombination. This injection effect can seriously limit the minimum fall time.

Figure A-10. Plot of Small Signal Degradation as a Function of Clock Frequency for Different Waveforms (Reference 8)

C.   Electrode Capacitance

The required characteristics for the clocking pulse drive circuits can be illustrated by estimating the effective capacitance "seen" by one of the clock drive lines. Let us assume in this example a 400 x 400 element array with a pixel size of 22.9 μm by 22.9 μm and that 3-phase, overlapping metal electrodes are used. (See the main body of the report for an explanation of the overlapping electrode structure.) Let us further assume that all charge packets are to be transferred from electrodes numbered 2 to the corresponding electrodes numbered 3 by a voltage pulse of 15 V applied to the electrodes 3, all in parallel. Because of the overlapping structure and the narrow separation there is a capacitive coupling from electrodes 3 to electrodes 2 and the same coupling from 3 to 1. These are in addition to the electrode to substrate capacitance, which is discussed in a preceding section, formed across the combination of oxide and depletion layers.

The "capacitor" coupling the electrodes is illustrated in Figure A-11(a). One part of this capacitor is approximated by a quarter of a cylindrical capacitor running the length of the electrodes (0.92 cm) with radii b and a for the outer and inner plates respectively. The other part is the parallel plate capacitor formed by the overlapping electrode. Let us assume the thickness of metal electrode and dielectric layers to be 0.3 μm and the width of overlap to be 0.3 μm. The ratio b/a would then be 2. The standard capacitor formulas are:

$$C_p = (0.3 \times 10^{-4} \; k \, \epsilon_o)/d \quad \text{farad/cm,} \tag{14}$$

$$C_C = (2\pi \; k \, \epsilon_o)/4 \; \ln(b/a) \quad \text{farad/cm,} \tag{15}$$

(a)

(b)
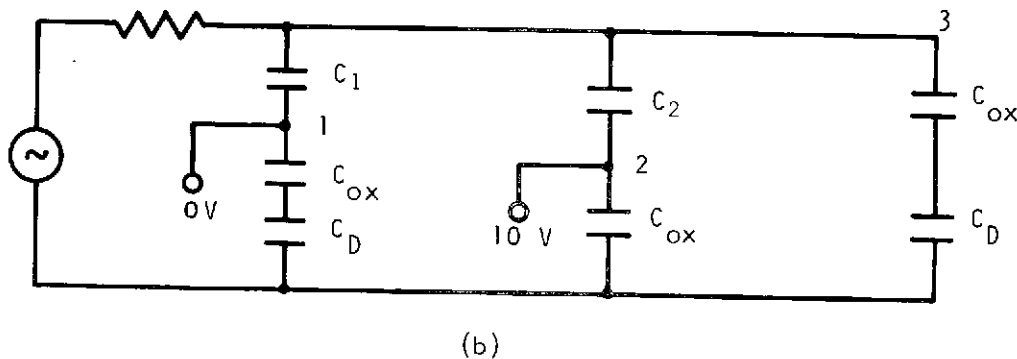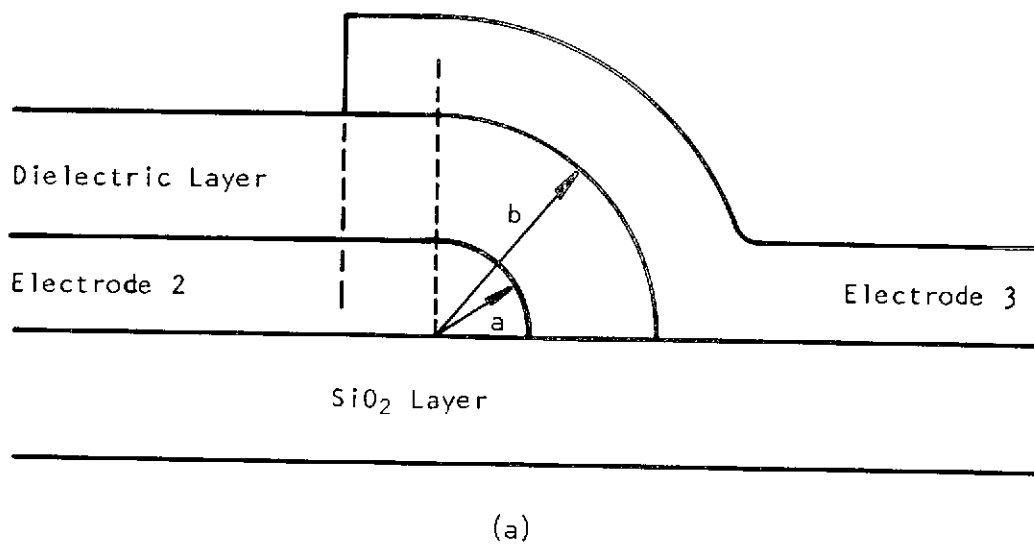
Figure A-11. Capacitance Seen by a Clock Drive Circuit

where k is equal to 8.6, the relative dielectric constant for the aluminum oxide, and ϵ_0 is the permittivity of free space equal to 8.85 x 10^{-14} farad-cm^{-1}. The total capacitance coupling electrode 3 to electrode 2 has been calculated to be 1 x 10^{-9} farad. There is a like capacitance to electrode 1.

The oxide layer capacitance as given in the preceding section for a 1200 Å thick oxide is approximately 2.8 x 10^{-8} farad per cm^2. When the depletion condition pertains, that is, an empty well and no inversion, the effective capacitance will be a fraction of the oxide layer capacitance, while for a full well the effective capacitance will be approximately the oxide capacitance. (See Figure A-6.) An electrode area is the electrode width multiplied by the channel width. For the pixel size assumed 7.4 μm and 17.8 μm are suitable values respectively for electrode and channel widths. With 16 x 10^4 elements the maximum electrode to substrate capacitance is 5.9 x 10^{-9} farad.

The network of capacitors to be driven by the phase 3 clocking source is illustrated in Figure A-11(b). Because electrodes numbered one will be held at a fixed potential, 0 V for example, the electrode to substrate capacitance of electrode 1 will not be "seen" by the phase-3 pulse. Similarly, electrode 2, which is in the occupied-well or inversion condition, will be held at a fixed voltage for a short time, 10 V for example. The phase-3 pulse rising from 0 V to 10 V will need to change the voltages across C_1, C_2, and the C_{ox} - C_D combination by 10 V. By using the formula

$$q = CV, \tag{16}$$

the charge that must be supplied to reach the full pulse voltage can be found to be 7.9 x 10^{-8} coulomb.

D. Charging Current

When data is being read out of the array at 10^4 pixels per second the master clocking frequency is 3 times this rate since three pulses are required to transfer a charge one pixel width. Hence, the allowed time to transfer charge packets from electrode 2 to electrode 3 is less than 3.3 x 10^{-5} second. In order for the voltages to be established early during this period so that there is sufficient time for efficient transfer of charge, let us, as an example, ask that the 7.9 x 10^{-8} coulomb be delivered in 3.3 x 10^{-6} second. If this charge were delivered as a uniform current pulse 3.3 μsec long, the current pulse amplitude would be 24 ma.

APPENDIX B

DESCRIPTIONS OF ALTERNATE CONFIGURATIONS

I. Introduction

One configuration, perhaps the simplest, of a charge-coupled Imager is discussed in Appendix A, and a second configuration is discussed in the main body of this report. Other modifications to the basic structure discussed in Appendix A have been proposed during the several years since the basic concept was reported (11). The modifications were often conceived to overcome some inherent limitation and sometimes to achieve certain performance goals. The most damaging limitations are those caused by the transfer inefficiency that limits the high frequency operation or the total number of elements in the device. A search for a solution to the transfer inefficiency problem apparently brought about the concept of a buried channel with its higher potential transfer rate and potential for eliminating surface state losses. A number of schemes, accounting for the largest portion of the number of different modifications, for providing directionality of charge transfer have been reported. Finally, there are several modes for scanning or reading out the data. These three types of modifications will be discussed in reverse order.

II. Scanning Modes

A. Full Frame

One type of scanning mode, which is called the full frame mode, is explained in Appendix A, Paragraph IV and, hence, is not explained here. This mode illustrates one example of a parallel to serial read out scheme.

B. Frame Store

In the simplest design of a charge transfer imaging device, several packets of stored charge are moved in unison across the light-sensitive region. This gives rise to image smear unless a shutter is used to cut off the incident light during readout of the integrated charge, or unless the charge is read out in a time very short compared with the integration time. A geometry that circumvents this problem for a line imaging device is shown in Fig. B-1. Charge packets are accumulated "under" storage electrodes that are separate from the lateral transfer electrodes. The charges are periodically transferred by way of the transfer region into the line readout region, which is shielded from the incident light. From the readout region the packets are transferred to the output diode. This is another example of a parallel-to-serial transformation which is readily achieved using charge coupling.

Fig. B-2 illustrates schematically one possible approach that may be used in making a three-phase area imaging device. (Reference 63) A 4 x 4-element imaging device is used as an example. The structure shown in the figure is divided into three functionally different areas: an optical integration section consisting of an array of 4 x 4 charge-coupled light-sensitive elements, a readout store consisting of an array of 4 x 3 charge-coupled storage elements of similar construction to the light-sensitive elements, and a line readout section consisting of a 4-element charge-coupled
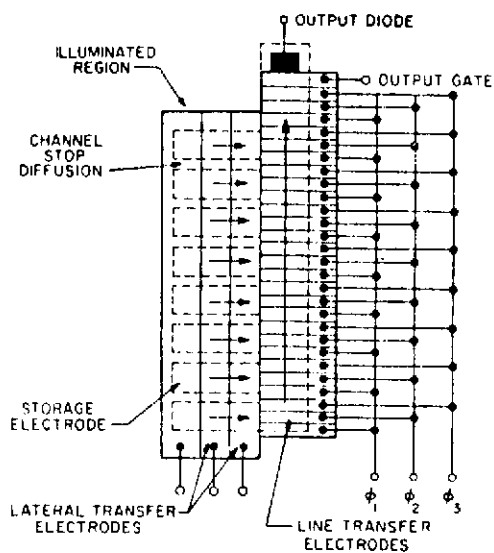
Figure B-1. Schematic Diagram of a Charge-Coupled Line
Imaging Device with Lateral Transfer to
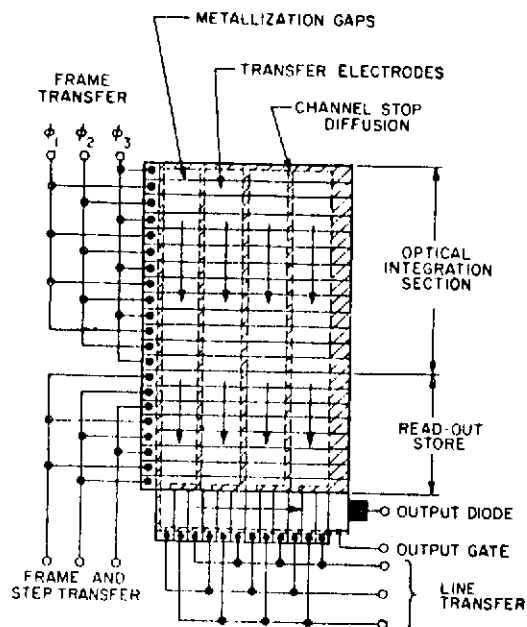Eliminate Shuttering (Reference 63)

Figure B-2. Schematic Diagram of a Charge-Coupled
Area Imaging Device
(Reference 63)

structure with an output diode at one end. The four vertical channels (charge transfer regions) in Fig. B-2 are isolated at the semiconductor surface by channel-stop diffusions. The electrodes in both the optical integration section and readout store run horizontally across all the transfer regions. The charge packets corresponding to the scene being imaged are accumulated in the 4 x 4-elements of the optical integration section during the time that the previous frame is being read out of the device from the read-out store. During the short time interval between readout of successive frames (which is equivalent to the vertical retrace time for a cathode-ray-tube monitor), all the electrodes effecting vertical transfer of charge are pulsed in a three-phase sequence, and the charge is moved into the nonilluminated storage region and line readout section. The lowest horizontal line of charge that was accumulated in the optical integration section is transferred into the line readout section, while the second lowest horizontal line is transferred into the lowest line of the readout store. The light integration region is now returned to the integrate mode. Frame readout is accomplished by transferring the charge pattern in the line readout section to the output diode, transferring another line of charge from the readout store into the line readout section, and then transferring this charge pattern to the output diode, and so on.

C.   Interlacing

Commercial broadcast TV presents the information contained in a full frame in two interlaced fields, each field containing half the total number of scan lines. This is done to reduce large area flicker in the display. Unless some kind of information reorganization is employed, as is anticipated in certain bandwidth reduction schemes, the pickup device in the camera has to present the information in the same interlaced timing format, that is, all the lines of one field must be read out consecutively, followed by all the lines of the other field.

Charge transfer devices are basically shift register structures that move a whole pattern of charge simultaneously. Depending on the readout organization in this type of image sensor, interlacing may not be achieved as simply as in x-y addressed arrays or in electron beam scanned targets.

In line-addressed structures (Fig. B-1), where the sequence of addressing the lines is determined by the driving circuitry, interlacing can be accomplished in a natural way. The frame transfer concept (Fig. B-2), on the other hand, does not naturally lead to an interlaced output, because the whole charge pattern has to move in unison. Proper interlacing can still be achieved by adding another storage area at the lower end of a frame transfer structure [Fig. B-3(a)]. This second store, having half the size of the imaging area, collects and stores every other line until they are read out with a second horizontal register and transmitted as the second field. The active area of such a device is now more than 2-1/2 times the physical size of the effective imaging section. Furthermore,

Figure B-3. Three Ways of Achieving a 2:1 Interlaced Readout from a Frame Transfer Imaging Structure (Reference 50)

the region of the first horizontal readout register would contain a highly complex electrode arrangement for electrical connections that requires at least a second level of metallization during device fabrication.

The frame transfer concept, however, can be adapted to yield a modified form of interlacing. (Reference 50) The serial readout section now consists of two identical shift registers [Fig. B-3(b)]. By shifting the data downward two steps at a time, a line pair is transferred from the store into these shift registers (one line in each register), which then are read out simultaneously into two separate diodes. One output is connected to the preamplifier and produces the video signal; the signal from the other diode is discarded. The second shift register could be replaced with one long diode. In one field, only the even lines are transmitted and all the odd ones are discarded. In the next field only the odd lines are transmitted. But discarding every other line means wasting half the signal. This results in a loss of light sensitivity, depth of field, or signal-to-noise ratio.

This loss of signal can be avoided, however, if in Fig. B-3(b) the output from the second diode, instead of being discarded, is electrically combined with the other one. Interlacing is then achieved by using different combinations of line pairs for the two fields. Such a mixing scheme results in a somewhat reduced vertical response for the highest spatial frequencies owing to the overlap between "lines" of subsequent fields. From the device point of view, the mixing scheme is prefereable since it requires a less complicated structure and does not result in a loss in sensitivity.

Since in each field only half the lines of a full frame are transmitted, it is sufficient to have only an equivalent number of storage lines. Thus, if the line pairs are combined before the transfer into the storage area, a considerable reduction in the number of necessary features in the store results.

The most economical way to do the mixing of adjacent lines is to do it during charge integration in the imaging area itself. Then the imaging section also needs only half the number of transfer elements in the vertical direction. A unit cell (a pixel) is now stretched over the vertical range corresponding to two adjacent scan lines of the display. The potentials on the electrodes during integration are sequenced differently for the two alternating fields. For the first field, the charge is accumulated under one set of electrodes. For the second field, the charge accumulates under a second set of electrodes displaced one-half pixel from the first set. This shifts the effective resolution cell boundaries and the center of charge collection by half a vertical cell dimension so as to match its position to the location of the corresponding scan line in the display [Figure B-3(c)].

This scheme can be readily adapted to any even-phase charge transfer structure. In a three-phase CCD in order to shift the resolution cell by 50 percent of its vertical dimension, one field has to be accumulated underneath two sets of electrodes jointly, while the other field is accumulated under the third set of electrodes. This scheme has been used both at Bell Telephone Laboratories and at TI, and appears to be quite satisfactory.

III. Electrode Structures

The 3-phase, single-level electrode structure, which is discussed in Appendix A, is the simplest transfer scheme providing directionality. However, tolerances that must be maintained during photolithographic processing require a too large minimum separation (3 μ) between electrodes to facilitate a rapid and efficient transfer of charge. The exposed oxide between electrodes is liable to adverse effects, for example, surface potential instability, caused by oxide ion contamination. Overlapping electrode structures seal the oxide surface, and thus prevent the oxide ion contamination effects. A relatively large number of different electrode structures have been reported, some of which are discussed in Reference 9. The 3-phase, overlapping, metal — $A\ell$-$A\ell_2O_3$-$A\ell$ — structure is discussed in the main body of this report and is not discussed here. (See References 46 and 23.) Other electrode structures are discussed in the following subsections.

A. Two-Phase and Four-Phase Double Level

1. Metal Electrodes.

A two-level metallization scheme may be used to fabricate either 4-phase or 2-phase CCD's. The structure is illustrated in figure B-4. In the 4-phase device, which uses an oxide either thermally grown on or deposited over every other electrode as an insulator between the electrodes, the direction of charge motion may be in either direction depending on the clocking signal sequence. However, in the 2-phase device, neighboring electrodes are connected in pairs and each pair is insulated from the neighboring pair by a deposited oxide. In such a structure, the upper and lower electrodes can be positioned so that their associated depletion layers overlap, thus allowing charge to move easily from one depletion region to the next. The direction of charge transfer is governed by the asymmetry; that is, the higher surface potential underneath the thicker oxide always causes the charges to transfer in one direction.

Several modifications to the overlapping metal electrode structure have been reported. Double layer metallization generally requires a more complex technology than single layer metallization, and a single layer technique which overcomes the photolithographic problems associated with the small electrode gaps necessary for CCD action would have much to commend it. A technique aimed at reducing the gaps has been described (Reference 4). The interelectrode gaps formed by this technique are approximately 0.1 μm, which is more than an order of magnitude smaller than those produced by conventional photolithographic techniques. An outline of the relevant parts of the fabrication process follows.

An insulating layer of silicon dioxide of approximately 1 μm thickness is grown or deposited on the surface of a silicon slice, and grooves are subsequently etched into this oxide to give the pattern shown in Figure B-5(a). The dimensions X and Y are not relevant to the discussion at the moment; typically they would be about 10 μm.

Figure B-4. Two CCD Structures Using Two-Level Metallization (Reference 61)

A second layer of oxide of approximately 0.1 μm thickness is grown or deposited on top of this structure to give a castellated oxide structure with the cross-section as shown in Figure B-5(b).

The silicon slice is now placed in an evaporation unit and aluminimized from a single source in the conventional way, with the following exception: the slice is mounted at an angle to the evaporation source so that discontinuities are created in the deposited aluminum layer wherever steps in the oxide shield part of the surface from the beam [see Figure B-5(c)]. These discontinuities (labeled C in the figure) form the required interelectrode gaps, the width of which will be in the same order as the heighth of the oxide step, that is, typically 0.1 μm. Owing to the castellated structure, each electrode is automatically separated from the underlying silicon by two different thicknesses of oxide [that is, A and B in figure B-5(c)]. This electrode arrangement resembles that shown in Figure B-5(d), although, of course, the two levels of metallization have been produced simultaneously in the structure being described. Moreover, the need for electrical connections between adjacent electrodes of Figure B-5(d) is now unnecessary. Since the connections are made automatically, the patterns of the photomasks used to form the electrode interconnections are simplified. In addition, the need to "dig down" to the level of the lower electrodes of Figure B-5(d) is obviated; fabrication complexity is reduced and chip area saved. This fabrication process is conceptually very much simpler than that for a double-layer metallization structure; this could have a significant effect on yields, particularly for CCD circuits with a large number of elements. It will be appreciated that the submicron interelectrode gaps do not require
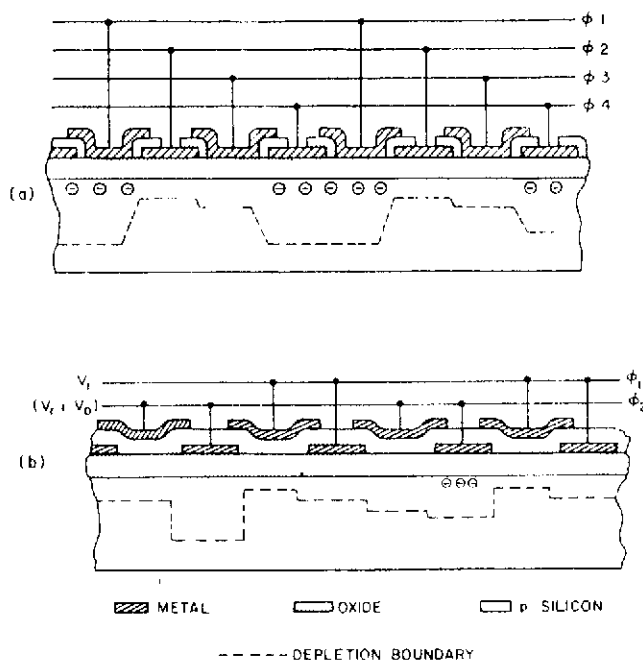
SiO$_2$ APPROXIMATELY 0.1 μM THICK

Si SUBSTRATE

(A)

APPROXIMATELY 0.1 μM

(B)

BEAM OF ALUMINUM ATOMS

(C)

A B C A B C A B

(D)

SiO$_2$

Si SUBSTRATE
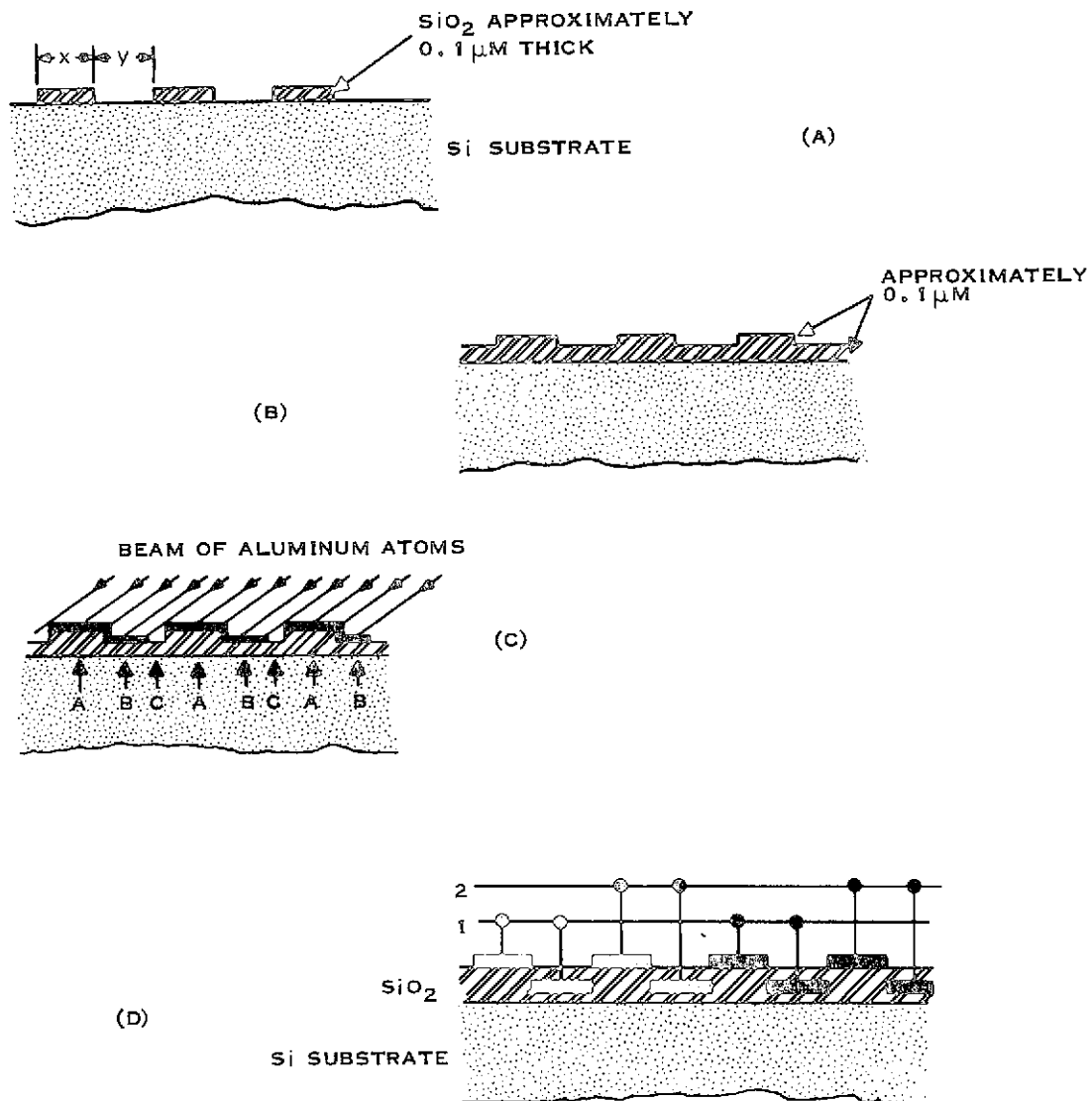
Figure B-5. Fabrication of a Double-Level Metal CCD Having Small Electrode Gaps

critical alignment or any special photolithographic techniques. Depositing metal from a single direction may adversely affect yield, however, as a result of step coverage problems in parts of the array where metal continuity is required. Furthermore, while this technique appears to have merit for linear arrays, it is difficult to employ in 2-dimensional arrays.

Another 2-phase, double-level, non-overlapping metal electrode structure having an essentially zero lateral spacing between gate electrodes has been designed and successfully fabricated. (Reference 7) The closely spaced metal gate isolation is provided by a self-aligned undercutting during etching of the SiO$_2$-Aℓ_2O$_3$ double-insulator system. The important features of the fabrication technique developed to implement this scheme are illustrated in Fig. B-6. A thick gate oxide (about 3500 Å) is grown first, followed by depositions of approximately 1000 Å of Aℓ_2O$_3$ and 2000 Å of SiO$_2$. This final layer of SiO$_2$ is patterned and used as an etch mask to permit

delineation of Al_2O_3 pads over the thick gate oxide as shown in Fig. B-6(a). Then the gate oxide is etched in the exposed regions to a thickness of about 1000 Å, using the Al_2O_3 as a mask, thereby producing the undercutting of approximately 2500 Å shown in Fig. B-6(b). This is followed by a second 500-Å Al_2O_3 deposition to seal the thin gate oxide, leaving the configuration of Fib. B-6(b). The next step is evaporation of Ti (~500 Å) and Pd (~1000 Å) over the entire wafer. Because the Ti-Pd metallization is thinner than the step height, there is no electrical connection between the metal pads on the thin and thick oxides, as shown in Fig. B-6(c). The two gate regions are connected at the desired points with a photoresist-masked electroless gold plating, producing the stepped electrode structure of Fig. B-6(d). In the final step, the Ti-Pd metallization is removed by etching everywhere except along the channels where it is masked by photoresist. The main disadvantages of this system are the fabrication complexity and the probability of a metal-to-metal short occurring for each centimeter of metallization length.

2. Doped Polysilicon-Metal.

A second type of double-level system is the doped polysilicon-SiO_2-Al, system which is used extensively in MOS device manufacture. The attractive feature of this technology is that the insulator between the polysilicon and the aluminum is a uniformly grown insulator rather than a deposited one. This growth of the insulator makes it possible to have a reasonably thin insulating layer of SiO_2 of high integrity, as opposed to deposited oxides, which never approach the integrity of a grown oxide.

A sealed-channel structure using the polysilicon-aluminum gate process has been described. (Reference 37). The gate construction allows fabrication of charge coupled structures with gate separation comparable to the thickness of the channel oxide. Also, the channel oxide is always covered by one of the metallizations. Another important advantage of the polysilicon process is that it provides a very simple method for the construction of 2-phase CCDs, which employ two thicknesses of channel oxide for the formation of asymmetrical potential wells needed for the unidirectional flow of signal.

The fabrication of the devices is illustrated in Figure B-7. The substrate used was 1.0–0.5 Ω cm n-type silicon on both (111) and (100) orientations. As shown at (a) the p+ diffusion and the field oxide were prepared following a conventional oxide p-type MOS process. Boron nitride deposited at 1000°C was used as the doping source for the p$^+$ diffusions. The field oxide was made as a combination of 7000 Å steam SiO_2 grown at 1100°C followed by 5000 Å deposited SiO_2. The next sequence of processing steps, as shown in Figure B-7(b), consisted of thermally growing an approximately 1000 Å
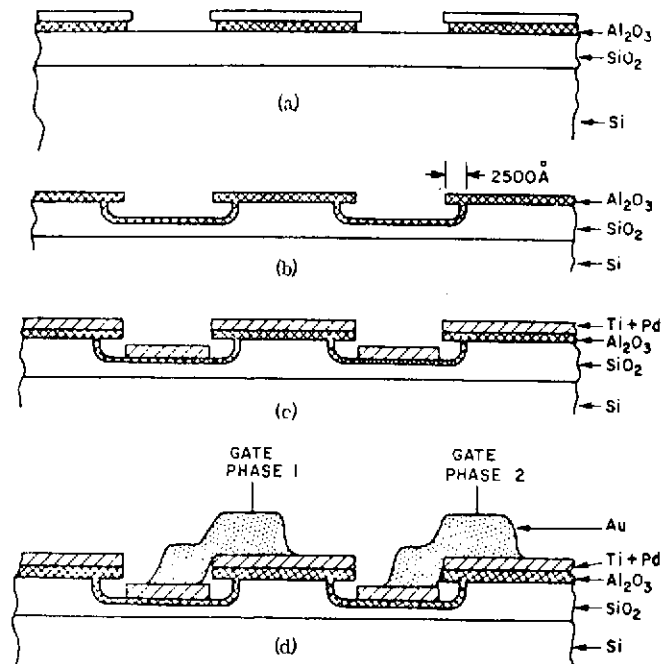

Figure B-6. Illustration of Undercut Isolation Process

thick channel oxide, depositing the polysilicon film, and patterning the polysilicon to form the gates. Then, as shown in Figure B-7(c), the polysilicon gates were insulated by a thermally grown oxide, and simultaneously the channel oxide for the aluminum gates was grown to the desired thickness. The initial devices having (111) orientation substrates were made with an aluminum gate channel oxide of 3000 Å, and the insulating oxide over the polysilicon gates was about 2500 Å. However, all of the devices that were made on substrates with (100) orientation were prepared with 2400 Å thick channel oxide for the aluminum gates. For these latter devices the insulating oxides for polysilicon gates was about 2000 Å. Finally, as shown in Figure B-7(d), the device structure was completed by opening contacts to the p+ diffusions and the polysilicon gates (not shown in the figure), depositing about 10,000 Å thick aluminum, and defining it into the aluminum gates. The main disadvantage in this fabrication scheme is the high resistivity of the polysilicon electrodes. This high resistivity will cause problems when clocking large arrays at high frequencies.

Figure B-7. Construction of 2-Phase CCD's in the Form of Polysilicon Electrodes Overlapped by Aluminum Electrodes (Reference 37)

B.   Ion-implanted Barriers, or Channels

Some of the inherent undesirable features of the simple non-overlapping gate structure can be circumvented by using the ion-implanted channel structure between electrodes. The charge-coupled device with non-overlapping gate structure has bare gate oxide between adjacent transfer gate electrodes. For this structure, the surface potential under the bare oxide must be externally controlled. The surface potential under the gap depends both on the charge condition of the bare oxide surface and on the fringing field of adjacent electrodes. The former depends critically on ambient conditions like humidity, through surface leakage. The fringing field of adjacent electrodes depends on the gap length, which must be less than 3 μm. In practice, however, fine-pattern photolithography gives rise to a serious yield problem for present day technology. For these reasons, the nonoverlapping gate structure presents many difficulties in practice.

The problems can be solved by forming buried channels under the gaps between the adjacent electrodes. (Reference 53) This device uses ion-implantation technology. The buried channels are formed by implanting opposite-type impurities in the silicon substrate about 0.4 μm deep. "Buried Channel" as used here refers to the implantation under the gap between electrodes shown in Figure B-8; hence, the meaning is different from the "buried channel" structure described in the main body of this report. Regardless of the surface potential under the gap, the charge moves to the potential minima through the buried channels under the gaps. Also, by implanting impurities of the same type as the substrate at the silicon surface, the inversion layer cannot be formed there.
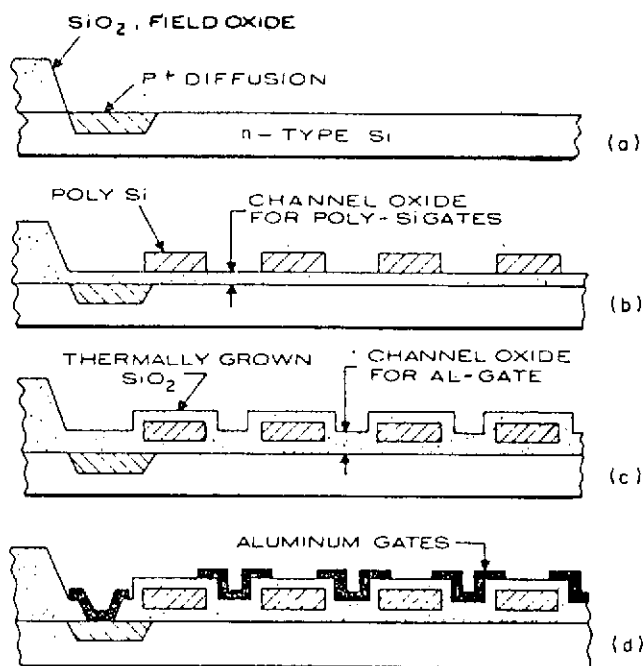
Furthermore, since there is no potential barrier under the gaps against charge transfer, the drift-aiding fringing field affects transferring charges more effectively, and high-voltage clock pulses are not necessary to ensure depletion at the surface under the gap.

Figure B-8 shows the cross section of a three-phase structure with gap buried channels. Gate oxide is grown about 0.14 μm thick on an n-type silicon substrate with (111) orientation. Polysilicon is used for the gate electrodes. After etching the polysilicon to define the gate areas used as the mask, the buried channels and channel stops at the silicon surface are formed by ion-implantation. The buried channels and the channel stops are respectively formed by implanting 5 x 10^{12}/cm^2 of boron about 0.4 μm deep and 10^{12}/cm^2 of some unspecified n-type dopant at the silicon surface.

The sheet resistance of the buried channel is about 8 kΩ/sq. The threshold voltage of the MOS gate structure is about -3 V. When all the gate electrodes are tied together, this device acts as an MOS-FET with a threshold voltage of about -3.5 V. If a conventional MOS-FET and an MOS-FET for which the source and drain are formed by buried channels are compared, their threshold voltages are found to be equal. In this type of device, there will be an inherent modulation of the channel length with signal amplitude causing a proportional loss of charge during charge transfer and a low transfer efficiency. This is similar to an effect in a similar device called the C4D (conductively connected charge-coupled device), which is not discussed here. (See Reference 9.)

Reference 39 discusses another type of 2-phase CCD which uses a non-uniform substrate doping to achieve directionality of transfer. (See also References 61 and 40.) This non-uniformity is obtained with a suitable pattern of ion-implantation. It allows considerable simplication of the metal and oxide patterns to the extent that only two non-overlapping electrodes per bit on a single thickness of insulator are needed, thereby substantially simplifying fabrication. In operation the two electrodes per bit are driven so that alternately one receives charge and the other gives it up. The necessary region of blocking potential is obtained with a line of immobile charge in the semiconductor implanted near the input end of each electrode. The immobile charge is chosen to have the same sign as the minority carriers.

A cross-section of a complete shift register is shown in Figure B-9. The device has a p-type substrate doped 10^{14}/cm^3 so that the information is carried by electrons near the surface. Boron is therefore chosen as the implanted material since it becomes negatively charged or ionized. A study of the potentials in this structure shows that the surface potential of the implanted region, for a shallow implant of 1.5 x 10^{12} cm^{-2} to be approximately 7 V less attractive to the electrons than the unimplanted region. The (input) diode at the left serves as a convenient source of minority carriers and is biased in a strong reverse bias (+15 V) except when injecting a packet of charge. The other (output) diode is always held in strong reverse bias. Variations in the voltage of a series resistor indicate the presence or absence of charge flowing into this diode.
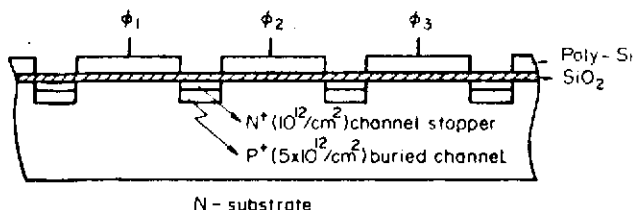

Figure B-8. Section Illustrating a 3-Phase CCD with
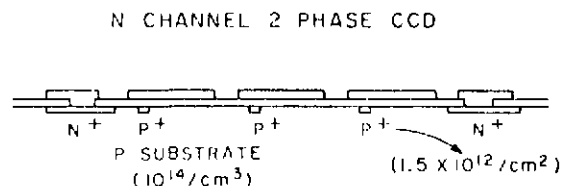Buried Channels in the Interelectrode Gaps

Figure B-9. Section Illustrating a 2-Phase CCD with
Implanted Barriers (Reference 39)

To move the charge from the first electrode to the second, the voltage on the first (and all other odd numbered electrodes) is reduced to 1 V. This makes the second electrode 9 V more attractive than the first. Therefore, all of the charge except that needed to fill the pocket at the left end of the second electrode can flow over the 7 V barrier to the second electrode. Once the flow has been completed, the voltages applied to the clock lines can be reversed and charge will advance another half bit. The major problem with this structure is the required precise registration of the implant with the edge of the electrode.

C.   Resistive Sea Gate Structure

For efficient transfer of carriers in the simple charge-coupled device, it is necessary that the silicon-silicon dioxide interface be depleted in the regions between adjacent gates. One way of achieving this condition, regardless of the type of the substrate doping, is to use an overlapping gate structure. However, the surface potential under the bare oxide between adjacent gate electrodes in a non-overlapping structure is extremely hard to control externally. Conceptually, we can reduce the gap length to be comparable to the oxide thickness and utilize the fringing field in a lowly doped substrate. In practice, however, gap lengths less than 3 μm give a serious yield problem with present day photomasking technology while the oxide thickness is usually only about 0.1 μm. As a result, gap lengths are typically 2.5 μm or more, and the surface potential under the gap depends primarily on Q_{ss}, the surface charge density, at the interface and on the charge condition of the bare oxide surface, both of which are not controllable externally. Since Q_{ss} is generally positive, it tends to accumulate electrons at the interface for p-channel device operation. Therefore, successful operation of p-channel charge-coupled devices with a nonoverlapping gate structure depends critically on the condition of the bare oxide, which is almost unpredictable. Although the surface leakage of the oxide layer will improve the situation by allowing the oxide surface to charge negatively, this depends critically on humidity, temperature, and device history. Furthermore, reliable operation of devices in hermetically-sealed packages is still a problem. The difficulty caused by the bare oxide can be solved by depositing a resistive material between the gate electrodes, thereby controlling the potential of the oxide surface. The device described here uses undoped polysilicon as the resistive sea material and doped polysilicon as the gate electrodes. (Reference 35.)

Figure B-10 shows the cross section of a three-phase structure using doped and undoped polysilicon. Undoped polysilicon is deposited at 850°C over a thin oxide of about 0.1-μm thickness. An oxide layer is then grown over the polysilicon and etched to define the gate areas. The exposed polysilicon is doped with boron in a predeposition furnace to form the highly conductive gate electrodes. The predeposition process is done as the last high-temperature process in fabricating the device to prevent shorts between the gates due to lateral diffusion. The resistivity of undoped polysilicon is about 10^5 Ω cm. For 0.5-μm thick polysilicon, this gives 2×10^9 Ω/sq sheet resistivity. Because of the high sheet resistivity, the driving power requirement will be extremely low. As an example, if the gate electrodes are 50 μm wide and separated by 5 μm, the power
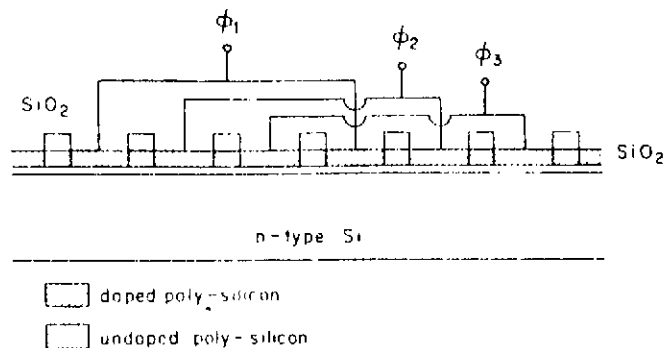

Figure B-10. Section Illustrating a p-Channel, silicon Electrode CCD Using Doped and Undoped Polysilicon (Reference 35)

dissipation in the undoped polysilicon will be less than 0.5 μW/gap for 10 V clock pulses. The time constant for charging this resistive region will be about 20 μsec, and hence the potential gradient will not be linear for operating frequencies above about 100 KHz. Nontheless, the potential will be controlled at some average of the clock voltages and will not be allowed to assume an arbitrary value. The principal disadvantages of the polysilicon resistive sea structure are the charging time constant required for satisfactory high frequency operation, and the extreme temperature dependence of the sheet resistivity of lightly-doped polysilicon.

IV. Channel Structures – Double-Junction CCD

The surface channel, charge-coupled device, as described in Appendix A, operates by moving minority carriers along the interface between a semiconductor and a dielectric layer with the application of voltage pulses to metal electrodes, the electrodes being insulated from the semiconductor by the dielectric. The characteristics of the transfer along the interface from the region near one electrode to a region near the next is determined by the minority carrier transport under the influence of their own potential, fringing fields, and diffusion, and by the trapping properties of interface states. Certain limitations are inherent in the transfer of charge along the interface, for example, a reduced charge transfer efficiency and an increase of noise. The limitations are such as to require the introduction electrically of a relatively large uniform "fat zero" into the array of wells before each exposure to light. The limitations may be appreciably reduced by the use of a buried channel structure, which is described in the main body of this report. This type of buried channel structure is not discussed in this Appendix. (However, see also References 32, 9, and 68.)

A third type of channel structure (in addition to the surface channel and the "simple" buried channel structure) is the double-junction CCD (DJCCD). (See Reference 49.) The array elements of the double-junction CCD for n-carriers have a p+-n-p-structure. The n-p⁻ junction corresponds to the equivalent part of a buried-channel CCD, and the doping profiles and electrical characteristics are very similar.

The conduction-band profile for a typical transfer electrode is shown in Fig. B-11, curve A. By applying a positive dc voltage to the output electrode, a totally depleted potential well is formed which can be used to store mobile charges. The well is enclosed by two reverse-biased junctions (hence the name double-junction CCD). Curves A, B, and C result when voltages of 0 V, +2 V, and -2 V, respectively, are applied to the p+-layer relative to the p⁻-substrate. These curves show that for the doping levels selected, more than 90 percent of the applied
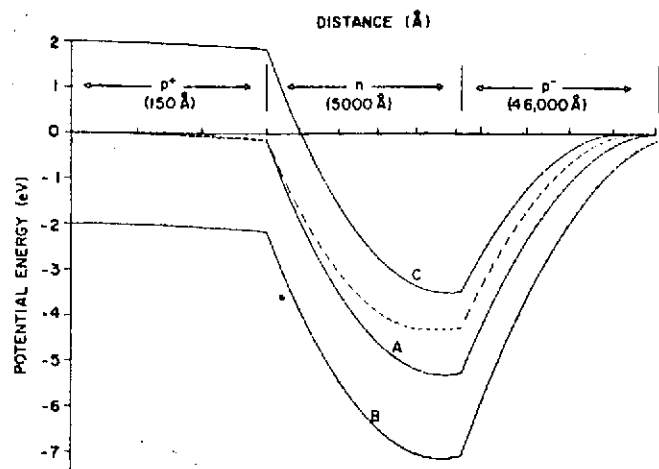

Figure B-11. Conduction Band Profile for a DJCCD Calculated Using the Abrupt Junction Approximation (Reference 49)

voltage is transferred to the depletion well minimum, which indicates that the efficiency of this device should be very high with respect to power consumption. The dashed curve results when electrons are present in the well at zero applied voltage. In this example, the number of electrons per unit surface area is assumed to be 10 percent of the number of donors within the n-layer per unit surface area. (The number of electrons is conveniently expressed relative to the number of donors since compensation occurs.) The figure indicates that for the filling level chosen, the well is still sufficiently deep to contain the mobile electrons, and, furthermore, that the well minimum does not change its location appreciably, thereby assuring good charge-transfer characteristics. Avalanche effects will not be present due to the low electric fields created. A low-voltage clock (≈ 2 V) should be sufficient to drive the device.

This structure is not known to have been operated. The leakage current of devices of this type may be high due to imperfect junctions. The lack of a gate oxide also places additional fabrication and operational constraints on the device.

A similar device called the Schottky-Barrier CCD (SBCCD) suffers from the same drawbacks.

APPENDIX C

ANALYSIS OF NOISE SOURCES

I.   Introduction

A charge-coupled imager (CCI) performs two functions with respect to the charge carriers generated by the absorption of photons: it stores discrete charge packets in the potential wells and at the appropriate time transfers the packets in sequence along each channel of the device to the output. Consequently, noise may be divided into transfer process (TP) noise and storage process (SP) noise. It is usually assumed that SP noise — shot noise for example — represent completely random and independent fluctuations between the charge packets. On the other hand, TP noise in adjacent packets is not independent since whatever charge is lost by one packet is gained by adjacent packets. Therefore, there is a correlation of TP noise fluctuations between adjacent charge packets; and this correlation must be taken into account when analyzing noise sources of CCI's.

The classification of noise into SP and TP sources seems to be rather arbitrary. For this reason, except for the need to remember that some noise may be correlated, the distinction is not carried further in this appendix.

II.   Shot Noise

In the CCI, signal charges are generated by an optical input; as a consequence, there is shot noise produced by random fluctuations in the arrival rate of photons. Also, the generation and recombination of carriers in a semiconductor are statistical processes so that any additional shot noise introduced by thermal generation-recombination processes will be added to the photon-produced shot noise. The average number of carriers, $N_{s,o}$, in a packet will therefore have a Poison distribution and the rms shot noise N_n will be the square root of that average number, that is,

$$N_n = (N_{s,o})^{1/2}. \tag{1}$$

Thermally introduced shot noise can be reduced by cooling the CCI, but photon noise will constitute a theoretical limit to the sensitivity of CCI's. The latter has been found not to be the limiting noise source in CCI's and will not be considered further herein.

III.   The Parallel RC Circuit

Thermal noise generated in the input resistance of the preamplifier is added to the output signal. One important aspect of a charge transfer device is that the signal charges may be brought to a very small output capacitance. An especially low noise contribution to the signal results in one instance from placing the preamplifier on the same chip with the CCI and in another instance by designing especially low noise circuits such as the precharge amplifier discussed in the main part of this report. Preset noise, as at the input to the precharge amplifier, is analyzed in the following paragraph.

Figure C-1 shows the circuit diagram of the configuration to be analyzed along with the noise equivalent circuit. The resistance R which represents the channel resistance of the precharge gate, is equivalent to a noise current source in parallel with an ideal resistance. The noise current produced is given by the standard equation:

$$\overline{i_n^2} = 4\,k\,T\Delta B/R, \tag{2}$$

where k is the Boltzmann constant, T is the temperature in K, and ΔB is the bandwidth. The voltage fluctuations across the RC network will depend upon its frequency characteristics. The mean-squared noise voltage per unit bandwidth is given by:

$$\overline{v_n^2} = \overline{i_n^2} \,/\, |G|^2, \tag{3}$$

where the conductance G is

$$G = (1/R) + j\omega C,$$
$$|G|^2 = (1/R^2)\,(1 + \omega^2 R^2 C^2). \tag{4}$$

In these last two equations, ω is equal to $2\pi f$, and f is the electrical frequency. The total mean-squared noise voltage is the integral over frequency of v_n^2:

$$\overline{V_n^2} = \int_0^\infty \overline{v_n^2}\,df$$

$$= (4kT/2\pi C) \int_0^\infty (1/RC)\left[(1/R^2 C^2) + \omega^2\right]^{-1} d\omega. \tag{5}$$

The value of the integral is given in several handbooks and is $\pi/2$. Then, the equation is

$$\overline{V_n^2} = k\,T\,/\,C. \tag{6}$$

The rms carrier fluctuation is

$$\overline{N_n} = (C\,\overline{V_n})\,/\,q = (k\,T\,C)^{1/2}\,/\,q \tag{7}$$

$$\approx 400\,(C_{pf})^{1/2}, \text{ at } T = 300K.$$

In Eq. (7), q is the electronic charge and C_{pf} is the capacitance in pf.

Note that while the resistance is the source of the fluctuations, its value does not affect the total carrier fluctuations. This is so because, while larger values of R increase the mean-squared noise voltage per unit
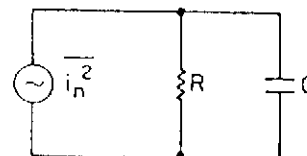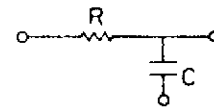

Figure C-1. Equivalent Circuit for a Resistance-Capacitance Input Impedance

bandwidth, they decrease the effective bandwidth by the same factor. A large capacitance reduces the bandwidth by $1/C$, therby reducing the noise voltage, but increases the number of carrier fluctuations for a given rms noise voltage by C; thus the C dependence.

The input capacitance of the on-chip preamplifier, the precharge amplifier, described in the main body of this report has been found to be approximately 0.07 pf. Obviously, the preamplifier noise is indeed quite low, $N_n \approx 105$ electrons.

IV. Electrically Introduced Noise

A "uniform" background charge density of 10 percent or more of a full well is generally required to reduce noises caused by carrier trapping in surface states. (Surface state noise is discussed in another section of this Appendix.) This background charge is usually introduced electrically as a "fat zero" in the wells; this would be a "slim zero" in the case of buried channel devices requiring an appreciably smaller background charge density. The charge must be introduced by way of the input capacitance, which is that of the potential well into which the charge is introduced. This capacitance may be of the order of 0.1 pf. Equation (7) applies; accordingly, the noise produced by the introduction of the fat zero is small.

V. Transfer Losses

The predominant source of TP noise in a surface-channel CCD is that due to interface state trapping. As signals are shifted along the register, the interface states are periodically filling and emptying. While on the average they fill and empty to the same levels each period (if the signal level is constant), there is a fluctuation about this average. This mean-squared fluctuation is given by $(\ln 2) \cdot (kT/q) N_{ss}A_g$ where N_{ss} is the density of fast interface states in $(cm^2-eV)^{-1}$ and A_g is the area of one gate. Since each packet gains charge from the packet ahead as well as losing charge to the trailing packet, a factor of 2 is required at each transfer; so after N_g transfers, the rms fluctuation due to interface state trapping is

$$\overline{N}_{n,\,trap} = [1.4\,(kT/q)\,N_{ss}N_gA_g]^{1/2}. \tag{8}$$

At low signal levels, this type of noise is expected to dominate for a large number of transfers, N_g.

Correlation of the noise between neighboring elements gives a $[1 - \cos \pi (f/f_n)]$ dependence so that the noise spectrum goes to zero as $f \to 0$. The electrical frequency corresponding to the Nyquist spatial frequency is f_n.

In surface channel devices, fast surface state noise is dominant and is the noise limiting the signal-to-noise ratio because all other noise can be reduced to appreciably smaller values. The buried channel device is free of the damaging effects of fast surface states; however, bulk state noise is present and a slim zero may be required.

VI. Fixed-Pattern Interference

A fixed pattern interference, independent of the noises that are accounted for theoretically in the preceding sections, may appear experimentally.

Fixed pattern interference would appear, for example, as a constant factor u, different from unity, that is multiplied by the quantity of charge Q that should appear in a given well and that would correctly represent the illuminance at the corresponding point in the scene being recorded. The factor u might be accounted for by a variation in the external quantum efficiency η_e which is the probability that an electron will appear in the well for each photon that is incident on the surface area "served" by that well. The variation from well to well may also appear as a differing additive constant, w, such as that caused by variations in dark current. The cause, or causes, of such variations whether local statistical variations in substrate and buried channel doping, depth or physical size of potential wells, or a localized defect, need to be investigated experimentally. Fortunately, whenever the data is to be processed, the value of u and w for each well can be determined in advance experimentally and a correction to the data made during data processing. The principal factor influencing fixed pattern interference has typically been observed to be dark current variations. These variations are dramatically reduced by cooling the device.

VII. Spectra of Noise Sources

In analyzing noise data, it is important to know how the charge transfer efficiency (CTE) affects the noise spectrum. In deriving the spectra for the different types of noise, we use the result that a CCD delay of m stages (one stage equals three transfers for a 3-phase device) having a loss per stage ϵ is equivalent to an ideal delay in series with a filter having transfer function given by

$$H(f) = \exp\left[-m\epsilon(1 - \cos 2\pi f/f_c)\right] .$$

(9)

Consider three sources of noise:

(1) Input noise, i.e., noise that is applied to the input and is attenuated by transfers through the entire device

(2) Leakage current noise, i.e., noise that is continuously being added to a charge packet as it travels down the device

(3) Surface state noise, i.e., noise which results from a variance in the amount of charge transferred each clock period.

With respect to each of these sources of noise, consider the fluctuation η (nT_c) in the number of charges in the charge packet that appears at the output during the nth clock period. Autocovariance, Q_η is defined by the equation

$$\langle \eta(nT_c) \, \eta[(n - m)T_c]\rangle \equiv Q_\eta \, (mT_c) ,$$

(10)

and spectral density $S_\eta(f)$ is defined by

$$S_\eta(f) \equiv \frac{1}{f_c} \sum_{m=-\infty}^{\infty} Q_\eta(mT_c)e^{-i2\pi m f/f_c} .$$

(11)

With these definitions, $S_\eta(f)$ has the significance of being the spectrum of the variance $\langle \eta^2 \rangle$ of the number of electrons per well:

$$\langle \eta^2 \rangle = \int_{-f_c/2}^{+f_c/2} S_\eta(f) \, df .$$

(12)

To relate $S_\eta(f)$ to the measured noise power density spectrum, it is necessary to multiply $S_\eta(f)$ by a frequency function that characterizes the output sampling. For example, if the output is impulse sampled, the frequency function characterizing the sampling is unity and $S_\eta(f)$ is proportional to the measured power density spectrum.

A. Input Noise

For a CCD requiring M transfers, the spectrum, $S_\eta(f)$, is given by

$$S_\eta(f) = \frac{\langle \xi^2 \rangle}{f_c} \exp[-2M\epsilon(1 - \cos 2\pi f/f_c)] ,$$

(13)

where $\langle \xi^2 \rangle$ is the variance in the fluctuation at the input. The normalized quantity $f_c S_\eta(f)/\langle \xi^2 \rangle$ is plotted in Figure C-2 as a function of frequency for different values of $M\epsilon$.

Also of interest is the total noise power at frequencies up to a frequency f. It is

$$P(f) = \int_{-f}^{+f} S_\eta(f')df',$$

(14

and this quantity normalized by $\langle \xi^2 \rangle$ is plotted in Figure C-3.

Figures C-2 and C-3 apply to fat zero noise or any other noise which is applied to the input.

B. Leakage Current Noise

The assumptions made in deriving the spectrum for this type of noise are that noise is being continuously and uniformly added to a charge packet as it travels down the shift register. The noise that is added to a charge packet after i transfers is attenuated by Eq. (9) with m = M - i; when contributions from all transfers are combined, the result is

$$S_\eta(f) = \frac{M\langle \xi^2 \rangle}{f_c} \left\{ \frac{1 - \exp[-2M\epsilon(1 - \cos 2\pi f/f_c)]}{2M\epsilon(1 - \cos 2\pi f/f_c)} \right\}$$
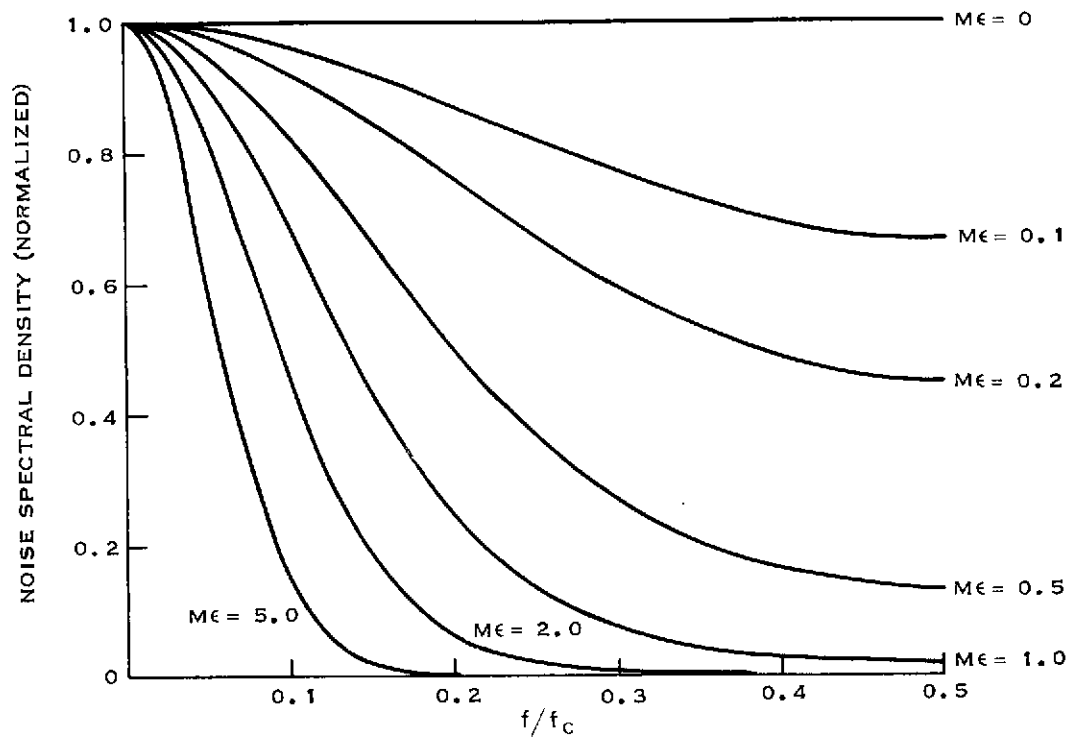
(15)

Figure C-2. Normalized Power Density Spectrum of Input Noise as Modified by Charge Loss in a CCD
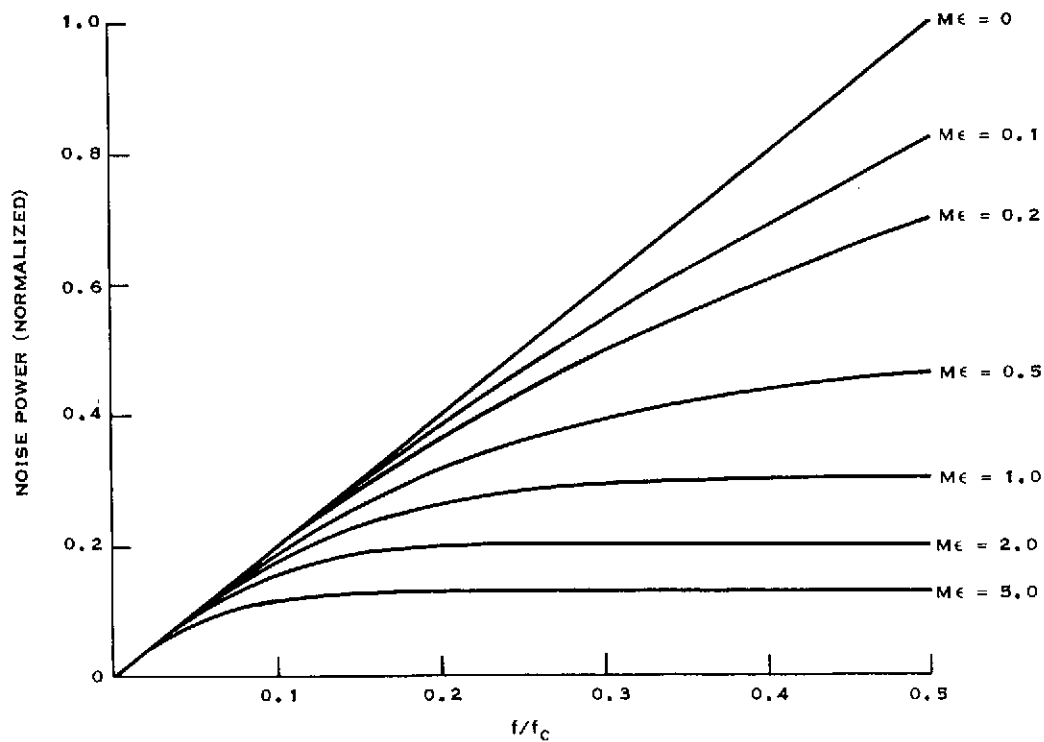

Figure C-3. Integral of the Curves in Figure C-2

where $\langle \xi^2 \rangle$ is the variance in the number of electrons that is added each transfer. The normalized quantity $S_\eta(f)\, f_c/(M\langle \xi^2 \rangle)$ is plotted in Figure C-4 and $P(f)/M\langle \xi^2 \rangle$ calculated from Eq.15 is plotted in Figure C-5. Figures C-4 and C-5 both show that leakage current noise is attenuated much less at high frequency than input noise. This is because, on the average, the former sees only half as many transfers as the latter.

C.   Surface-State Noise

Noise caused by fast surface states can be treated by writing

$$\eta(nT_c) = \sum_{i=1}^{M} (\xi_{i,n} - \xi_{i,n+1}),\tag{16}$$

where the $\xi_{i,n}$ are statistically independent random variables which represent the fluctuation in the nth charge packet in passing from the jth to the $(j+1)$th stage. The autocovariance of η can be calculated from Eq. (16) to be

$$Q\eta(mT_c) = M\langle \xi^2 \rangle(2\delta_{m,0} - \delta_{m,1} - \delta_{m,1}).\tag{17}$$

By substituting Eq. (17) into Eq. (11), one can obtain the equation:

$$S_\eta(f) = \frac{\langle \xi^2 \rangle}{\epsilon f_c} \left\{ 1 - \exp\left[-2M\epsilon(1 - \cos 2\pi f/f_c)\right] \right\}.\tag{18}$$

In Figure C-6 the normalized quantity $f_c S_\eta(f)/(2M\langle \xi^2 \rangle)$ is plotted. When $\epsilon = 0$, Eq. (18) reduces to the familiar expression:

$$S_\eta(f) = \frac{2M\langle \xi^2 \rangle}{f_c} (1 - \cos 2\pi f/f_c).\tag{19}$$

The normalized power $P(f)/(2M\langle \xi^2 \rangle)$ plotted in Figure C-7 shows that, by restricting the bandwidth at the CCD output, the surface state noise can be reduced dramatically. For example, for $M\epsilon = 0$, halving the bandwidth reduces the surface state noise power to 0.18 of its full bandwidth value.

The quantity$\langle \xi^2 \rangle$ can be calculated in terms of device parameters by the relation

$$\langle \xi^2 \rangle = A_g kT\, N_{ss} 2\, \log_e(2),\tag{20}$$

where A_g is the CCD gate area, k is Boltzmann's constant, T is the absolute temperature, and N_{ss} is the surface state density.
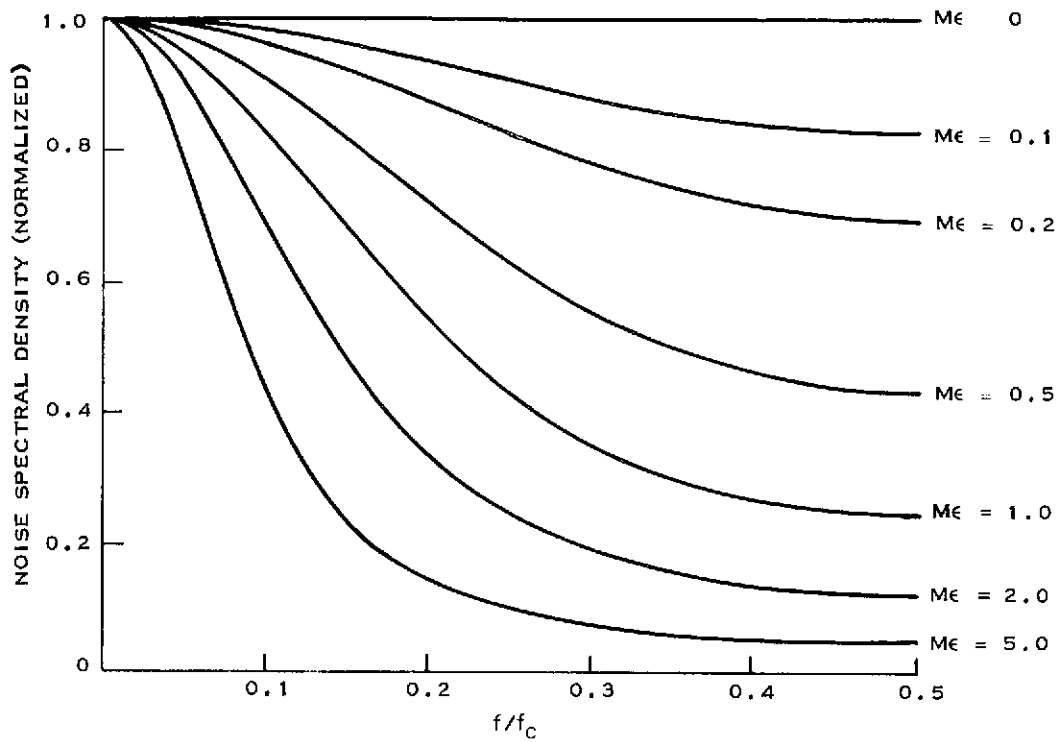
Figure C-4. Normalized Power Density Spectrum of Leakage Noise as Modified by Charge Loss in a CCD
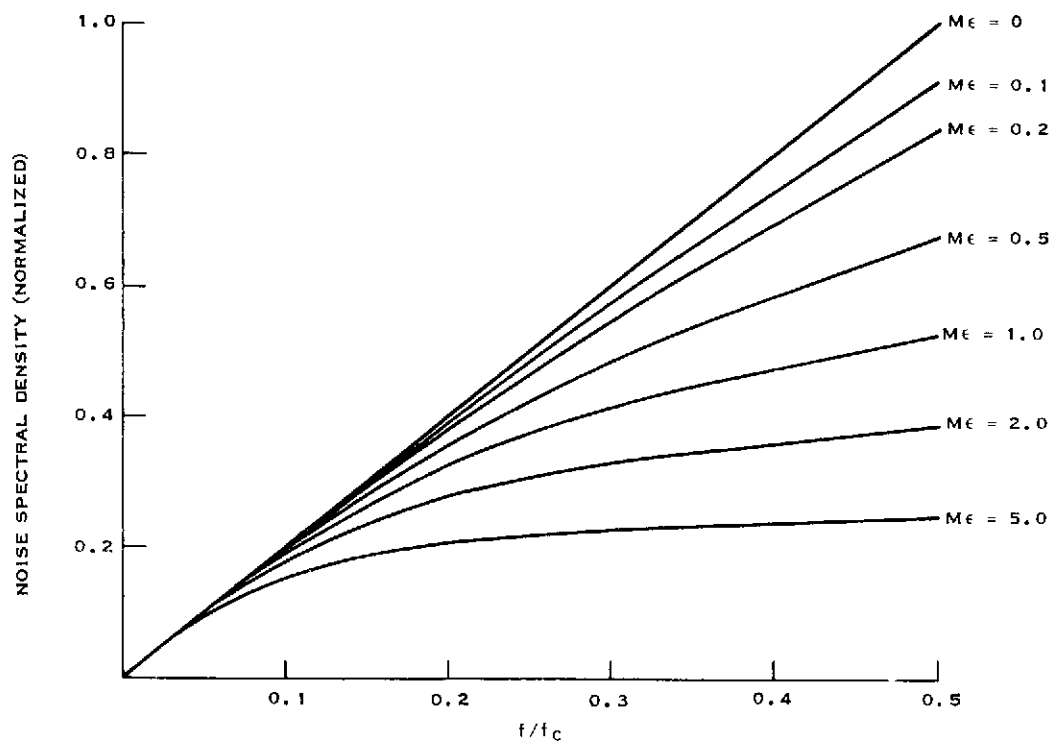

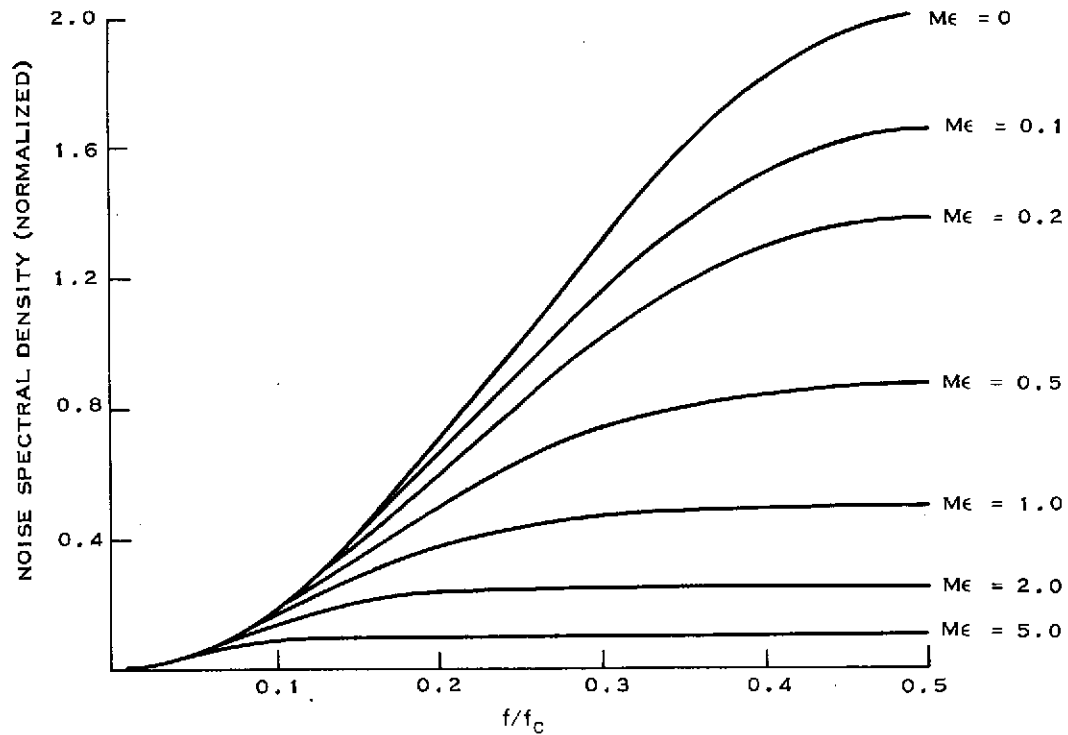Figure C-5. Integral of the Curves in Figure C-4

Figure C-6. Normalized Power Density Spectrum of Surface State Noise as Modified by Charge Loss in a CCD
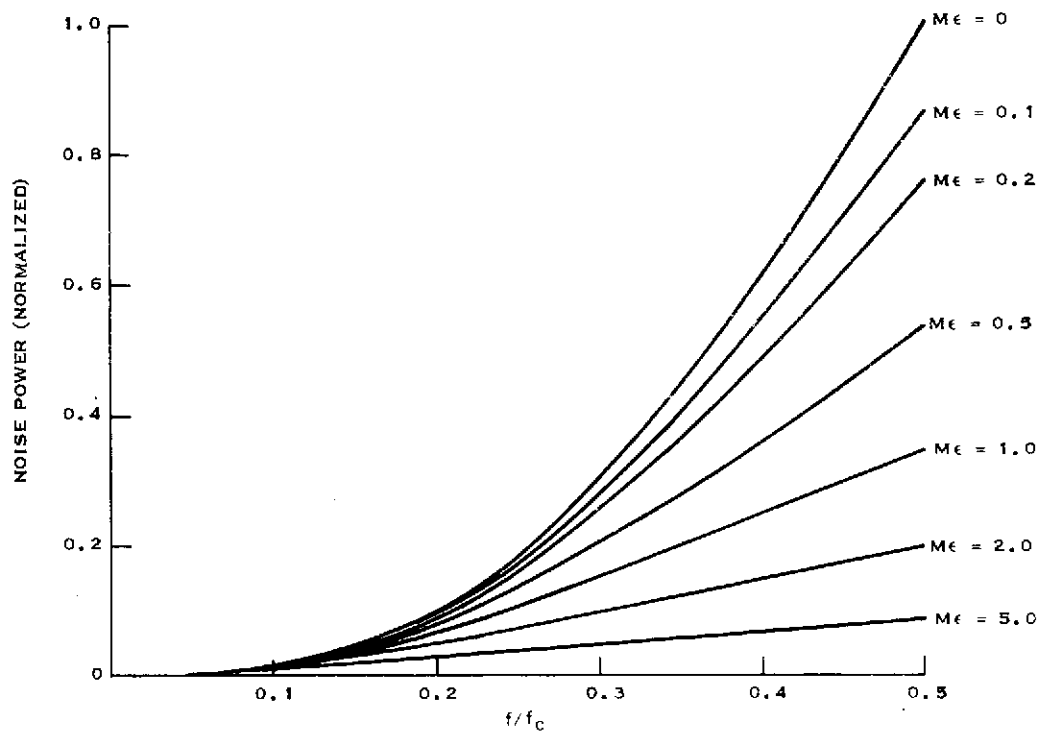

Figure C-7. Integral of the Curves in Figure C-6

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